

Model Name: GA-Z77X-UD3H

1.2

SHEET

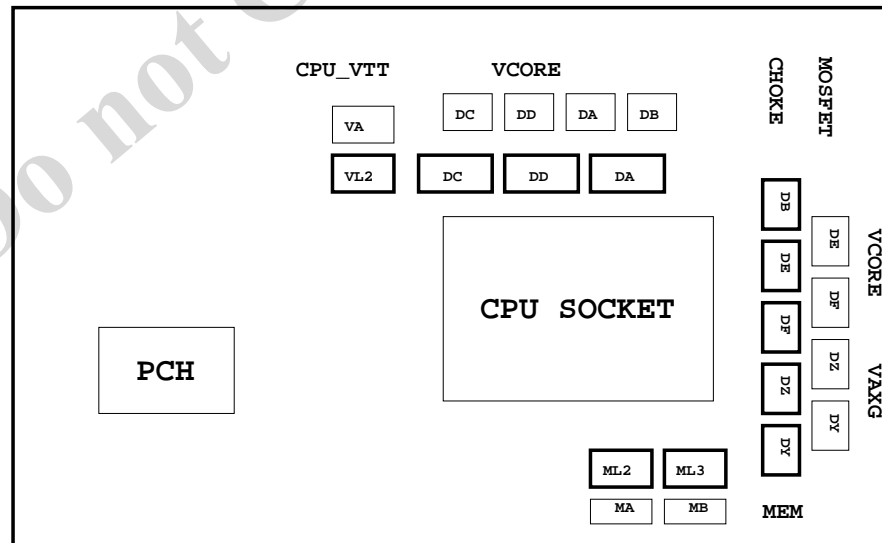
TITLE

| | |
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| 02 | BOM & PCB MODIFY HISTORY |
| 03 | BLOCK DIAGRAM |
| 04 | CPU_LGA1155-A |
| 05 | CPU_LGA1155-B |
| 06 | CPU_LGA1155-C |
| 07 | DDR III CHANNEL A |
| 08 | DDR III CHANNEL B |
| 09 | PCH_FDI,DMI,USB,PCIE |
| 10 | PCH_DP_HDMI_DVI_DAC,CLK BUFFER |
| 11 | PCH_HOST,SATA,PCI |
| 12 | PCH_GPIO,CTRL,AUDIO |
| 13 | PCH_PWR,GND |
| 14 | PCI EXPRESS*16 SLOT |
| 15 | PCI EXPRESS*8 SLOT |
| 16 | PCI EXPRESS*16/*8 SWITCH |
| 17 | PCI EXPRESS*1 SLOTS X3 |
| 18 | PCI EXPRESS*4 SLOT / SWITCH |
| 19 | IT8892 PCIE to PCI BRIDGE |
| 20 | PCI SLOT |
| 21 | DP / HDMI / DVI Connector |
| 22 | mSATA Connector |
| 23 | Dual BIOS , TPM |
| 24 | VT2021 |
| 25 | REAR AUDIO JACK |
| 26 | VCORE PWM_IR3567-1 |
| 27 | VCORE PWM_IR3567-2 |

SHEET

TITLE

| | |
|----|-------------------------------|
| 28 | DDR_15V & CPUVTT PWM_IR3570-1 |
| 29 | DDR_15V & CPUVTT PWM_IR3570-2 |
| 30 | DISCRETE POWER 1 |
| 31 | DISCRETE POWER 2 |
| 32 | I/O IT8728F |
| 33 | USB3_ESATA , KB/USB3, -PHOT |
| 34 | F_PANEL , F_USB , F_USB3 |
| 35 | ATX POWER, CLOCK GEN |
| 36 | HWM, FAN CTRL |
| 37 | Atheros 8151 |
| 38 | ESATA SE9172 |
| 39 | 80PORT / PWR SW / OV NCT3933 |
| 40 | VIA VL800 |
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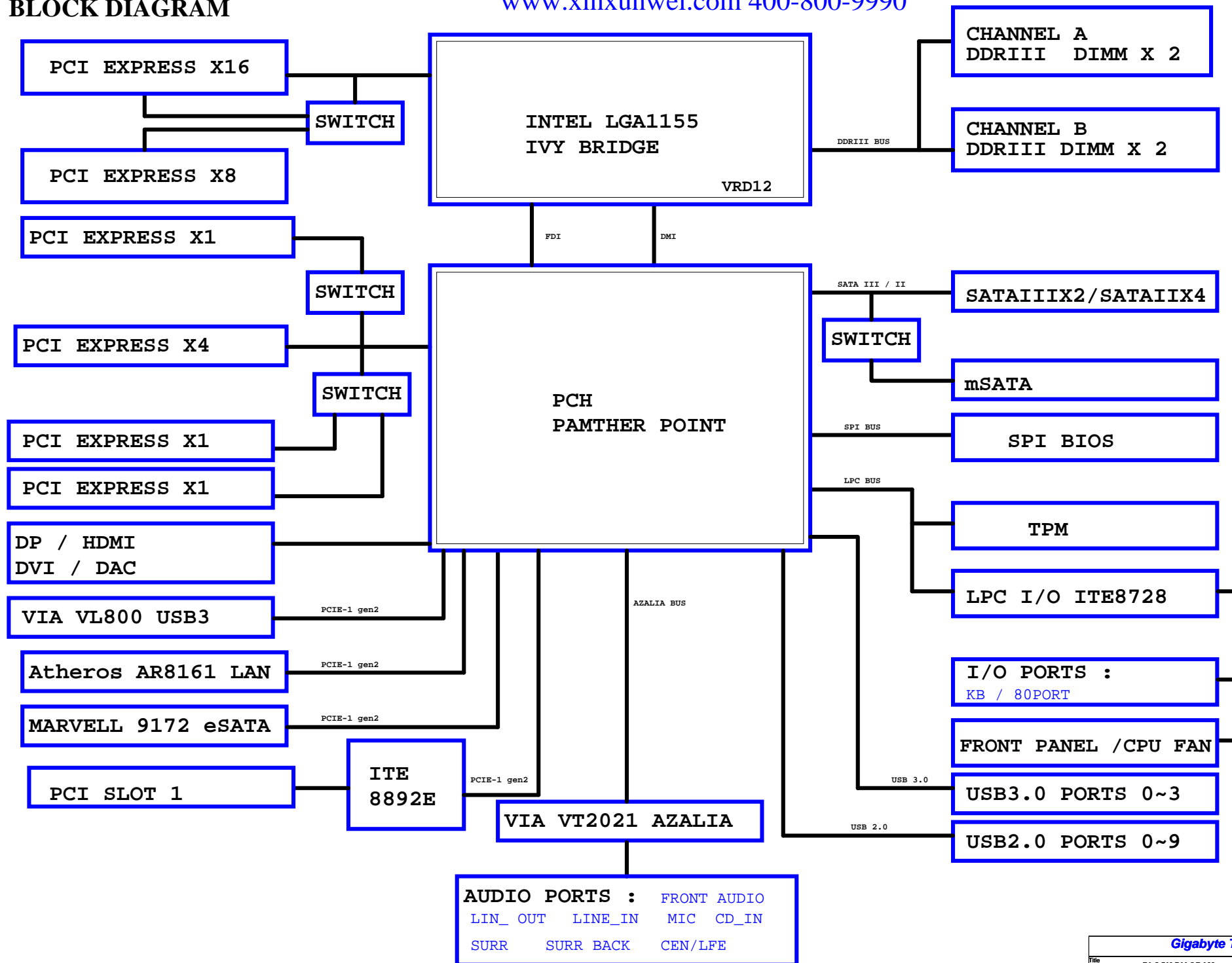


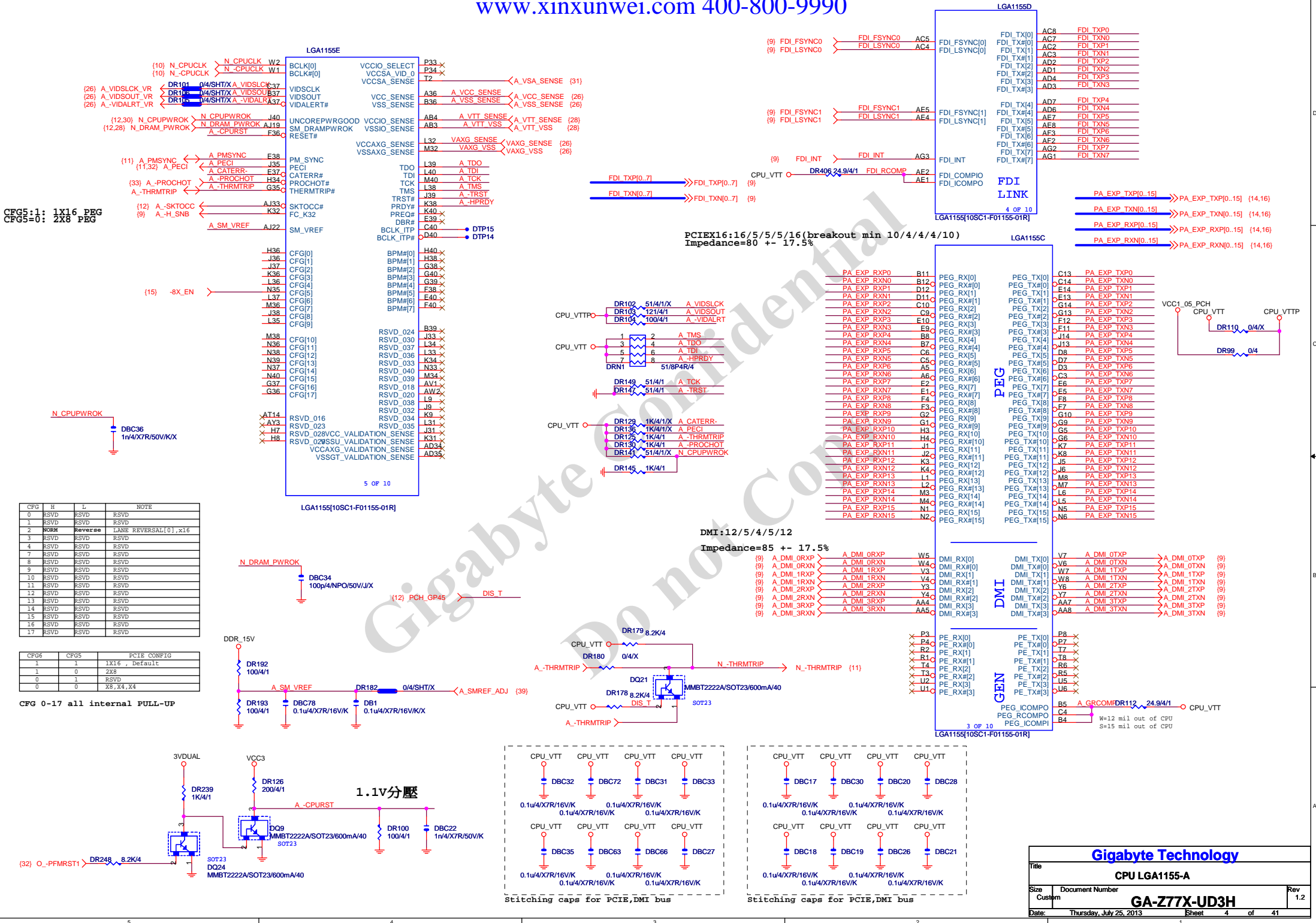
Gigabyte Technology

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|-------------|-------------------------|--------------|---------|
| Title | | | |
| Cover Sheet | | | |
| Size | Document Number | GA-Z77X-UD3H | Rev 1.2 |
| Custom | | | |
| Date: | Thursday, July 25, 2013 | Sheet 1 | of 41 |

BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990





LGA1155A

| | | | | |
|--------|------|-----------|-----|---------|
| M_AA0 | AV27 | SA_MA[0] | AK3 | M_DQSA0 |
| M_AA1 | AY24 | SA_MA[1] | AK2 | M_DQSA0 |
| M_AA2 | AW24 | SA_MA[2] | | |
| M_AA3 | AW23 | SA_MA[3] | | |
| M_AA4 | AV23 | SA_MA[4] | AJ3 | M_DA0 |
| M_AA5 | AT24 | SA_DQ[1] | AJ4 | M_DA1 |
| M_AA6 | AT23 | SA_MA[5] | AJ3 | M_DA2 |
| M_AA7 | AU22 | SA_MA[6] | AL4 | M_DA3 |
| M_AA8 | AV22 | SA_MA[7] | AJ2 | M_DA4 |
| M_AA9 | AT22 | SA_MA[8] | AJ1 | M_DA5 |
| M_AA10 | AV28 | SA_MA[9] | AL2 | M_DA6 |
| M_AA11 | AU21 | SA_MA[10] | AL1 | M_DA7 |
| M_AA12 | AT21 | SA_MA[11] | | |
| M_AA13 | AW32 | SA_MA[12] | AP3 | M_DQSA1 |
| M_AA14 | AU20 | SA_MA[13] | AP2 | M_DQSA1 |
| M_AA15 | AT20 | SA_MA[14] | | |
| | | SA_MA[15] | | |

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|-----|---------|---------|------|---------|
| (7) | M_SWEA | M_SWEA | AW29 | SA_WE# |
| (7) | M_SCASA | M_SCASA | AV30 | SA_CAS# |
| (7) | M_SRASA | M_SRASA | AU28 | SA_RAS# |

| | | | | |
|-----|--------|--------|------|----------|
| (7) | M_SBA0 | M_SBA0 | AY29 | SA_BS[0] |
| (7) | M_SBA1 | M_SBA1 | AW28 | SA_BS[1] |
| (7) | M_SBA2 | M_SBA2 | AV20 | SA_BS[2] |

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|-----|--------|--------|------|--------|
| (7) | M-CSA0 | M-CSA0 | AU29 | SA_CS# |
| (7) | M-CSA1 | M-CSA1 | AV32 | SA_CS# |
| (7) | M-CSA2 | M-CSA2 | AW30 | SA_CS# |
| (7) | M-CSA3 | M-CSA3 | AU33 | SA_CS# |

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|-----|---------|---------|------|-----------|
| (7) | M_CKEA0 | M_CKEA0 | AV19 | SA_CKE[0] |
| (7) | M_CKEA1 | M_CKEA1 | AT19 | SA_CKE[1] |
| (7) | M_CKEA2 | M_CKEA2 | AU18 | SA_CKE[2] |
| (7) | M_CKEA3 | M_CKEA3 | AV18 | SA_CKE[3] |

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|--|----------|------|-----------|
| | M_ODT_A0 | AV31 | SA_ODT[0] |
| | M_ODT_A1 | AU32 | SA_ODT[1] |
| | M_ODT_A2 | AU30 | SA_ODT[2] |
| | M_ODT_A3 | AW33 | SA_ODT[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

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|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

| | | | | |
|-----|----------|----------|------|----------|
| (7) | M_DCLKA0 | M_DCLKA0 | AY25 | SA_CK[0] |
| (7) | M_DCLKA1 | M_DCLKA1 | AW25 | SA_CK[1] |
| (7) | M_DCLKA2 | M_DCLKA2 | AU24 | SA_CK[2] |
| (7) | M_DCLKA3 | M_DCLKA3 | AW26 | SA_CK[3] |

DDR_0

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LGA1155[10SC1-F01155-01R]

LGA1155B

| | | | | |
|--------|------|-----------|-----|---------|
| M_AA0 | AK24 | SB_MA[0] | AH7 | M_DQSB0 |
| M_AA1 | AM20 | SB_MA[1] | AH6 | M_DQSB0 |
| M_AA2 | AM19 | SB_MA[2] | | |
| M_AA3 | AK18 | SB_MA[3] | AG7 | M_DB0 |
| M_AA4 | AP19 | SB_MA[4] | AG8 | M_DB1 |
| M_AA5 | AP18 | SB_MA[5] | AJ9 | M_DB2 |
| M_AA6 | AM18 | SB_MA[6] | AJ8 | M_DB3 |
| M_AA7 | AL18 | SB_MA[7] | AG5 | M_DB4 |
| M_AA8 | AN18 | SB_MA[8] | AG6 | M_DB5 |
| M_AA9 | AY17 | SB_MA[9] | AJ6 | M_DB6 |
| M_AA10 | AN23 | SB_MA[10] | AJ7 | M_DB7 |
| M_AA11 | AU17 | SB_MA[11] | | |
| M_AA12 | AT18 | SB_MA[12] | AM8 | M_DQSB1 |
| M_AA13 | AR26 | SB_MA[13] | AL8 | M_DQSB1 |
| M_AA14 | AY16 | SB_MA[14] | | |
| M_AA15 | AV16 | SB_MA[15] | | |

| | | | | |
|-----|---------|---------|------|---------|
| (8) | M_SWEB | M_SWEB | AR25 | SB_WE# |
| (8) | M_SCASB | M_SCASB | AK25 | SB_CAS# |
| (8) | M_SRASB | M_SRASB | AP24 | SB_RAS# |

| | | | | |
|-----|--------|--------|------|----------|
| (8) | M_SBA0 | M_SBA0 | AP23 | SB_BS[0] |
| (8) | M_SBA1 | M_SBA1 | AM22 | SB_BS[1] |
| (8) | M_SBA2 | M_SBA2 | AW17 | SB_BS[2] |

| | | | | |
|-----|--------|--------|------|--------|
| (8) | M-CSB0 | M-CSB0 | AN25 | SB_CS# |
| (8) | M-CSB1 | M-CSB1 | AN26 | SB_CS# |
| (8) | M-CSB2 | M-CSB2 | AT26 | SB_CS# |
| (8) | M-CSB3 | M-CSB3 | AT26 | SB_CS# |

| | | | | |
|-----|---------|---------|------|-----------|
| (8) | M_CKEB0 | M_CKEB0 | AU16 | SB_CKE[0] |
| (8) | M_CKEB1 | M_CKEB1 | AY15 | SB_CKE[1] |
| (8) | M_CKEB2 | M_CKEB2 | AW15 | SB_CKE[2] |
| (8) | M_CKEB3 | M_CKEB3 | AV15 | SB_CKE[3] |

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|-----|----------|------|-----------|
| (8) | M_ODT_B0 | AL26 | SB_ODT[0] |
| (8) | M_ODT_B1 | AP26 | SB_ODT[1] |
| (8) | M_ODT_B2 | AM26 | SB_ODT[2] |
| (8) | M_ODT_B3 | AK26 | SB_ODT[3] |

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|-----|----------|----------|------|----------|
| (8) | M_DCLKB0 | M_DCLKB0 | AL21 | SB_CK[0] |
| (8) | M_DCLKB1 | M_DCLKB1 | AL22 | SB_CK[1] |
| (8) | M_DCLKB2 | M_DCLKB2 | AK20 | SB_CK[2] |
| (8) | M_DCLKB3 | M_DCLKB3 | AN21 | SB_CK[3] |

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|-----|----------|----------|------|----------|
| (8) | M_DCLKB0 | M_DCLKB0 | AL21 | SB_CK[0] |
| (8) | M_DCLKB1 | M_DCLKB1 | AL22 | SB_CK[1] |
| (8) | M_DCLKB2 | M_DCLKB2 | AK20 | SB_CK[2] |
| (8) | M_DCLKB3 | M_DCLKB3 | AN21 | SB_CK[3] |

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|-----|----------|----------|------|----------|
| (8) | M_DCLKB0 | M_DCLKB0 | AL21 | SB_CK[0] |
| (8) | M_DCLKB1 | M_DCLKB1 | AL22 | SB_CK[1] |
| (8) | M_DCLKB2 | M_DCLKB2 | AK20 | SB_CK[2] |
| (8) | M_DCLKB3 | M_DCLKB3 | AN21 | SB_CK[3] |

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|-----|----------|----------|------|----------|
| (8) | M_DCLKB0 | M_DCLKB0 | AL21 | SB_CK[0] |
| (8) | M_DCLKB1 | M_DCLKB1 | AL22 | SB_CK[1] |
| (8) | M_DCLKB2 | M_DCLKB2 | AK20 | SB_CK[2] |
| (8) | M_DCLKB3 | M_DCLKB3 | AN21 | SB_CK[3] |

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|-----|----------|----------|------|----------|
| (8) | M_DCLKB0 | M_DCLKB0 | AL21 | SB_CK[0] |
| (8) | M_DCLKB1 | M_DCLKB1 | AL22 | SB_CK[1] |
| (8) | M_DCLKB2 | M_DCLKB2 | AK20 | SB_CK[2] |
| (8) | M_DCLKB3 | M_DCLKB3 | AN21 | SB_CK[3] |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

| | | | |
|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

| | | | |
|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

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|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

| | | | |
|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

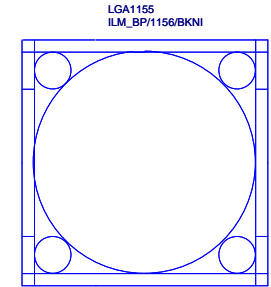
| | | | |
|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

| | | | |
|-----|------------|-----|--------|
| (8) | M_VREF_DQB | AH1 | FC_AH1 |
| (7) | M_VREF_DQA | AH4 | FC_AH4 |

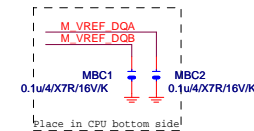
DDR_1

2 OF 10

LGA1155[10SC1-F01155-01R]



Need check the new CPU ME



Gigabyte Technology

CPU LGA1156-B

| | | |
|--------|-------------------------|---------------|
| Size | Document Number | Rev |
| Custom | GA-Z77X-UD3H | 1.2 |
| Date: | Thursday, July 25, 2013 | Sheet 5 of 41 |



DDR_15V

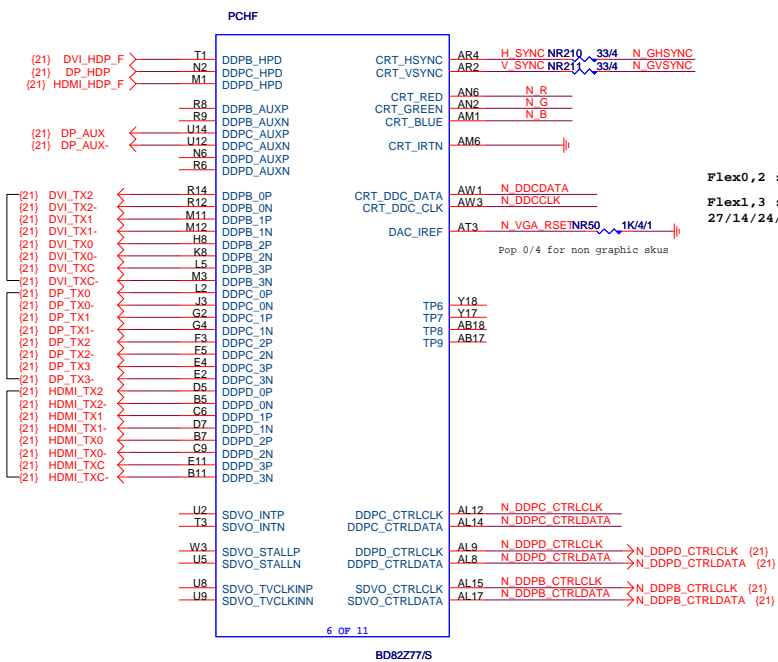


DDRVTT

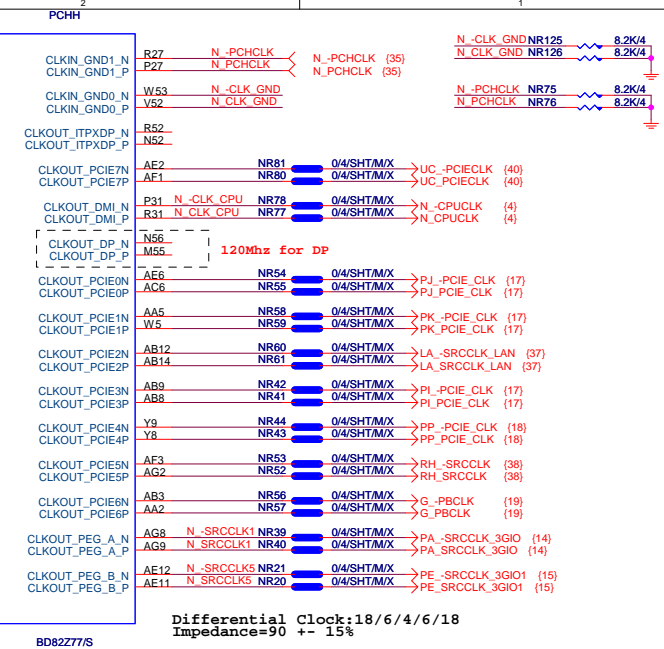
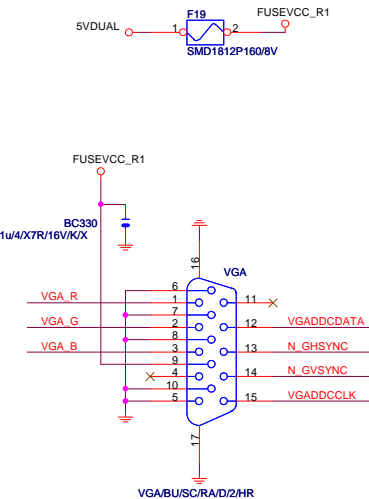
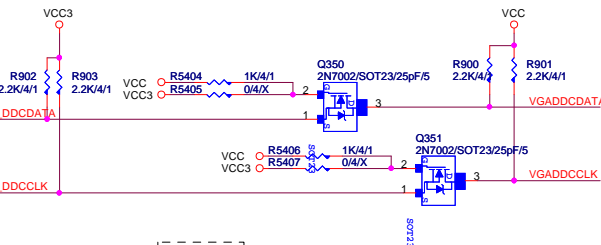
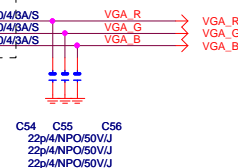
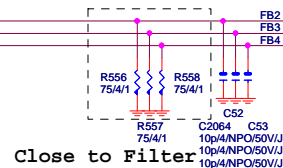
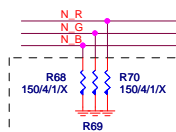
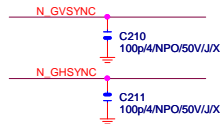
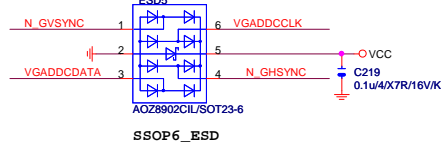
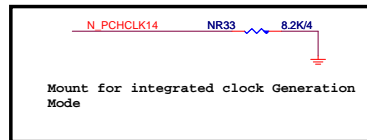
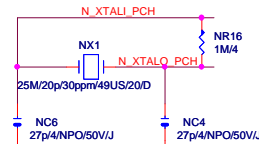
MBC32







Flex0,2 : 33MHz
Flex1,3 : 27/14/24/48/25MHz

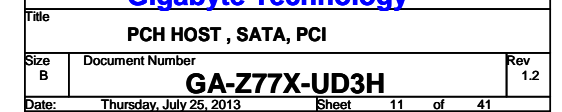


Differential Clock:18/6/4/6/18
Impedance=90 +- 15%

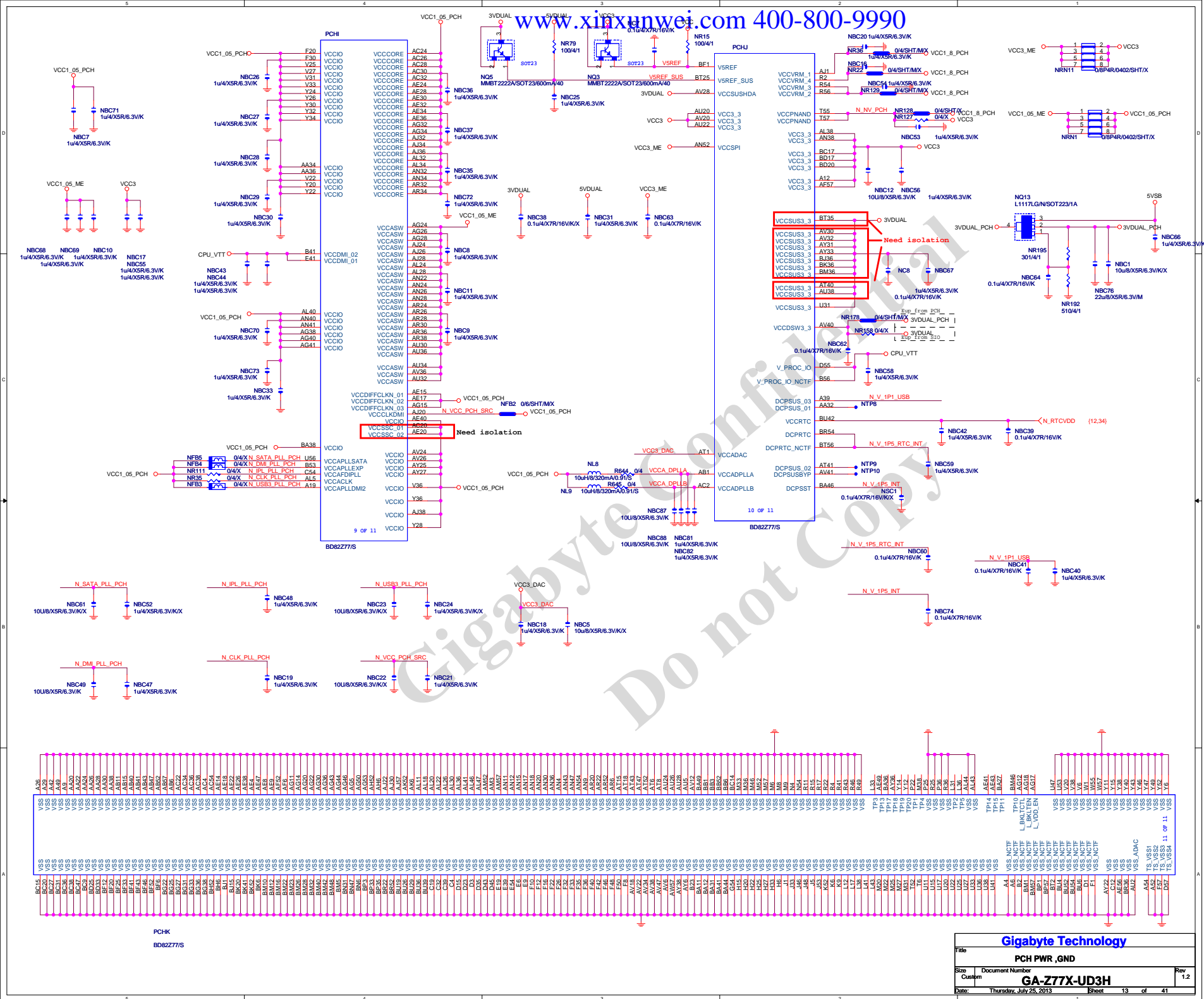
Gigabyte Technology

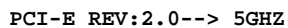
PCH DISPLAY ,CLK BUFFER

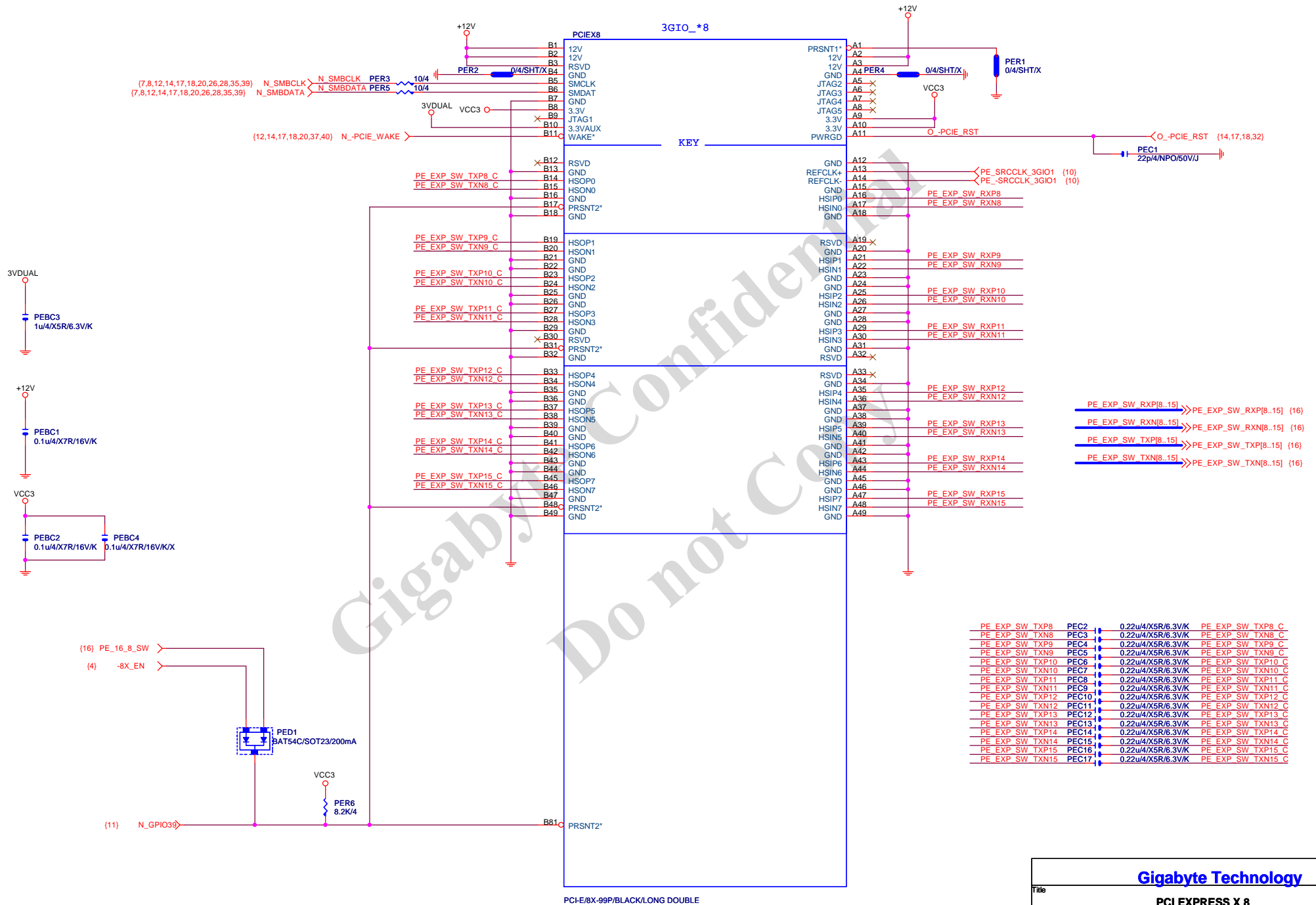
Title: PCH DISPLAY ,CLK BUFFER
Size: Custom Document Number: **GA-Z77X-UD3H** Rev: 1.2
Date: Thursday, July 25, 2013 Sheet: 10 of 41







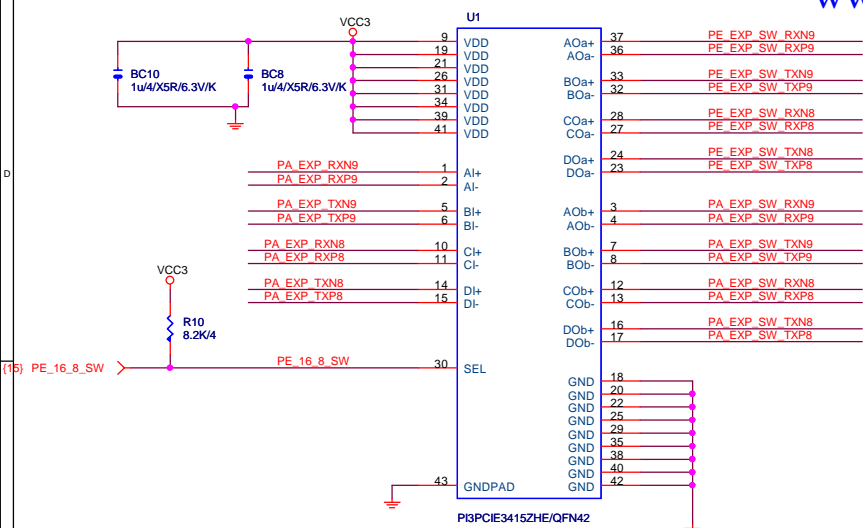




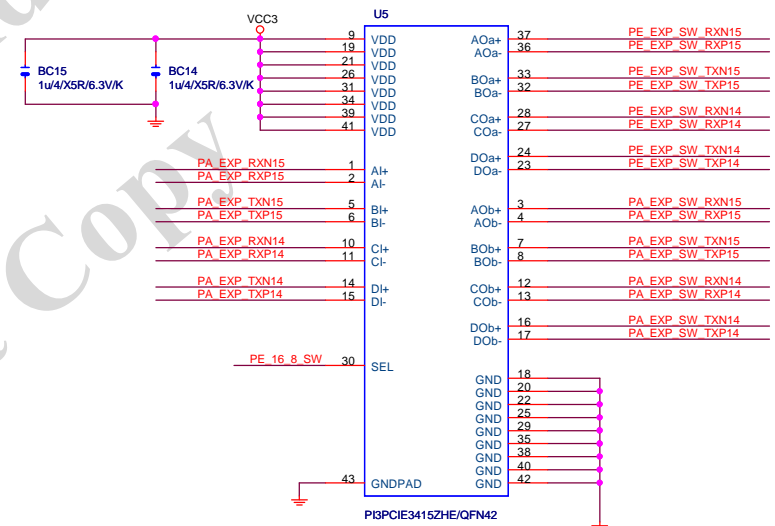
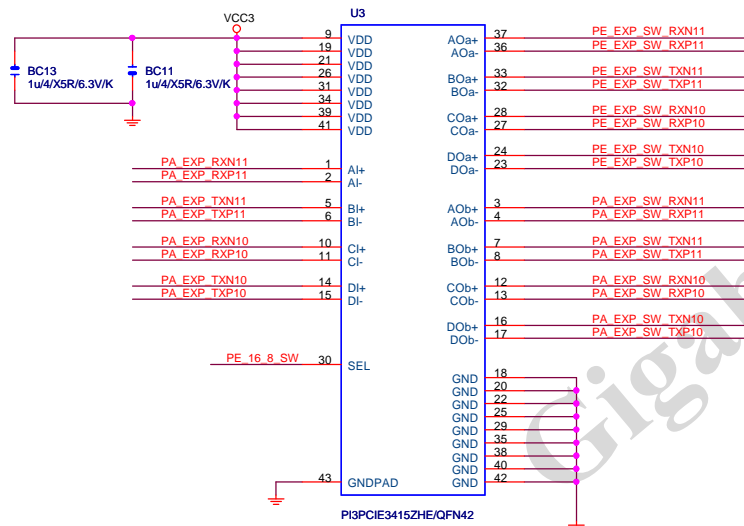
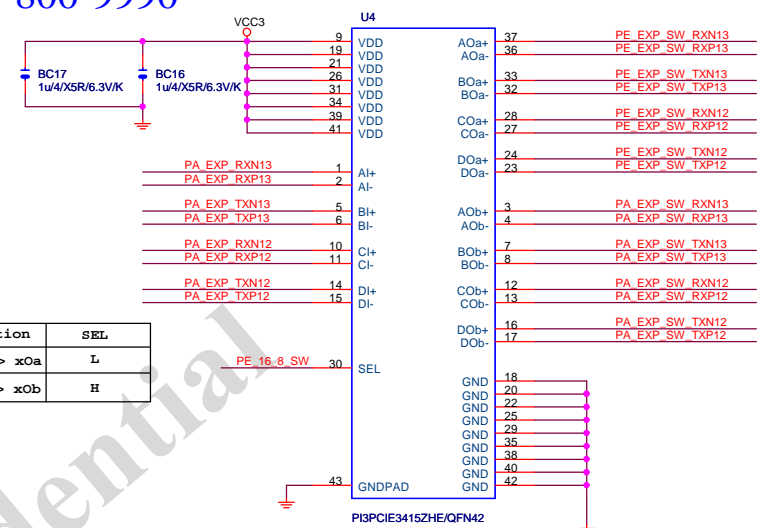
PCI-E/8X-99P/BLACK/LONG DOUBLE

Gigabyte Technology

| | | | |
|--------|-------------------------|-----------------|----------|
| Title | | PCI EXPRESS X 8 | |
| Size | Document Number | GA-Z77X-UD3H | |
| Custom | | Rev 1.2 | |
| Date: | Thursday, July 25, 2013 | Sheet | 15 of 41 |

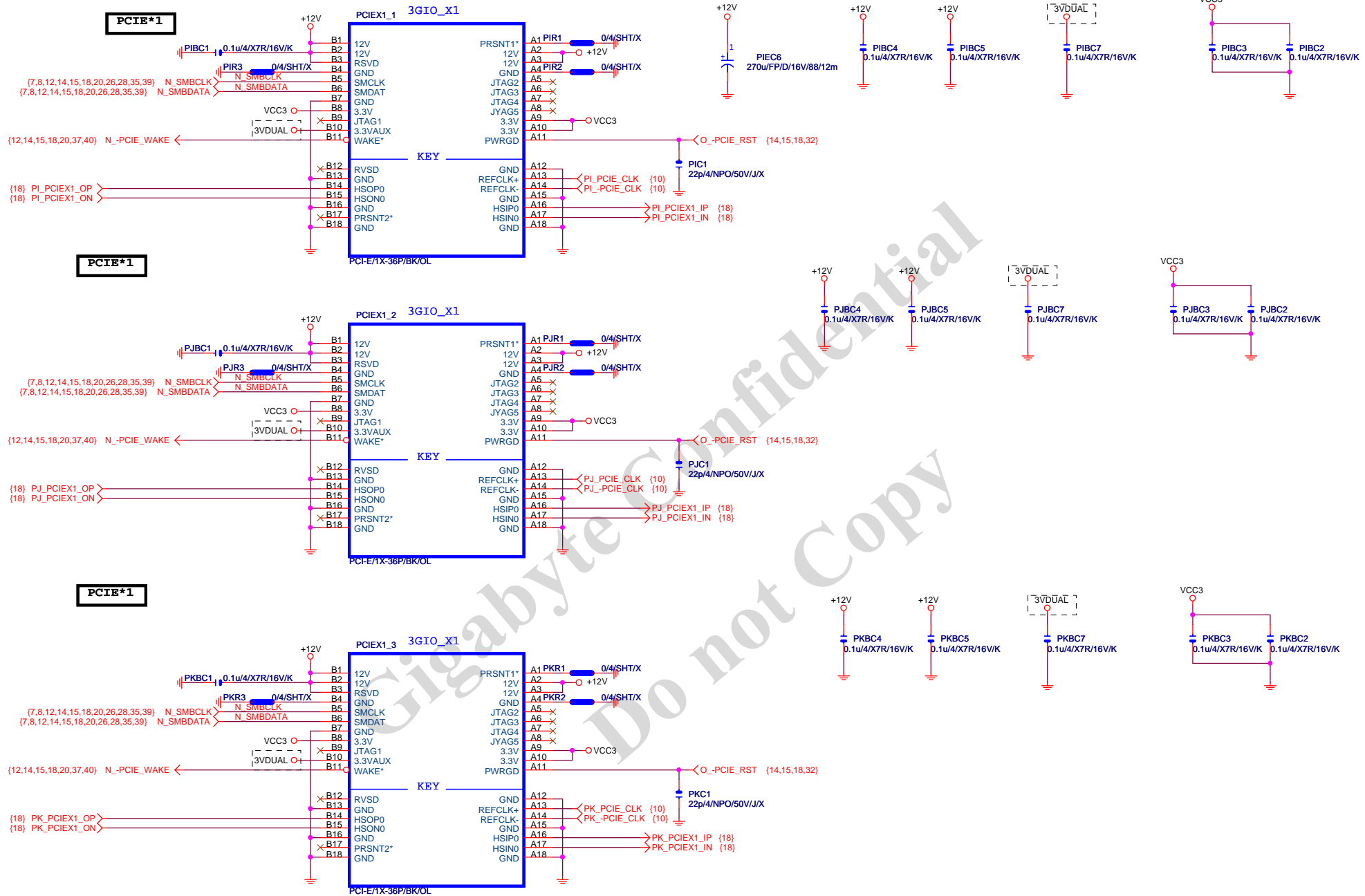


| Function | SEL |
|-----------|-----|
| xI--> xOa | L |
| xI--> xOb | H |



PA EXP SW RXP[8..15] >> PA_EXP_SW_RXP[8..15] (14)
 PA EXP SW RXN[8..15] >> PA_EXP_SW_RXN[8..15] (14)
 PA EXP SW TXP[8..15] >> PA_EXP_SW_TXP[8..15] (14)
 PA EXP SW TXN[8..15] >> PA_EXP_SW_TXN[8..15] (14)
 PE EXP SW RXP[8..15] >> PE_EXP_SW_RXP[8..15] (15)
 PE EXP SW RXN[8..15] >> PE_EXP_SW_RXN[8..15] (15)
 PE EXP SW TXP[8..15] >> PE_EXP_SW_TXP[8..15] (15)
 PE EXP SW TXN[8..15] >> PE_EXP_SW_TXN[8..15] (15)
 PA EXP RXP[0..15] >> PA_EXP_RXP[0..15] (4,14)
 PA EXP RXN[0..15] >> PA_EXP_RXN[0..15] (4,14)

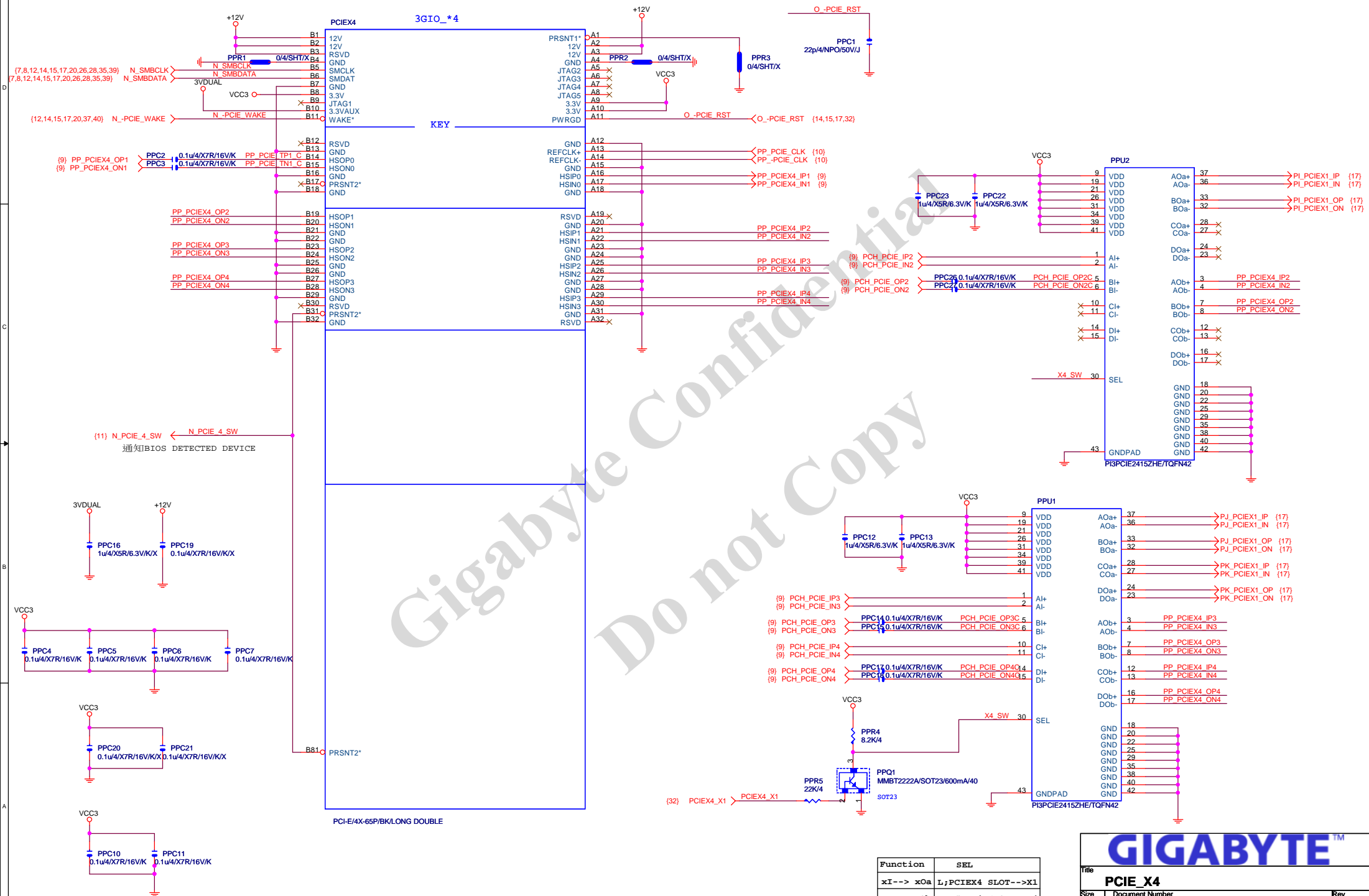
PA EXP TXP[0..15] >> PA_EXP_TXP[0..15] (4,14)
 PA EXP TXN[0..15] >> PA_EXP_TXN[0..15] (4,14)



Gigabyte Technology

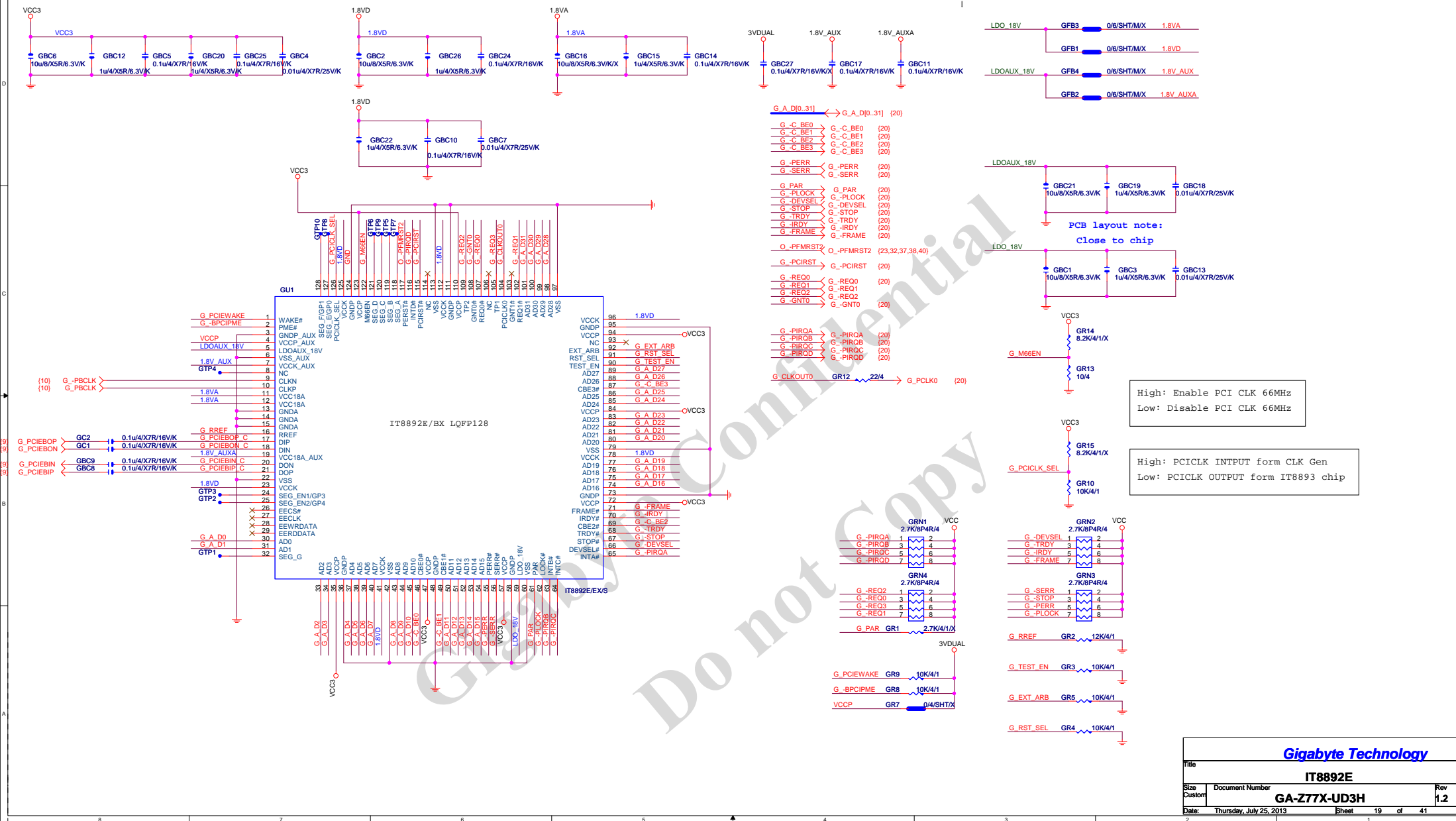
| | | | |
|--------|-------------------------|--------------|---------------|
| Title | | | PCIE_X1 1,2,3 |
| Size | Document Number | Rev | |
| Custom | | GA-Z77X-UD3H | |
| Date: | Thursday, July 25, 2013 | Sheet | 17 of 41 |

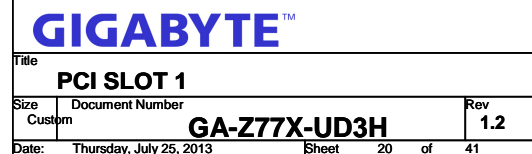
PCIE*4

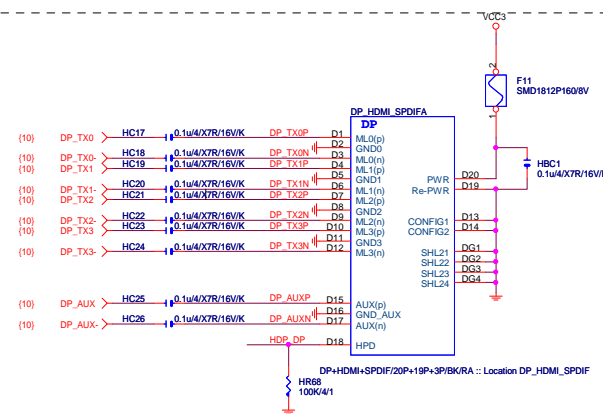
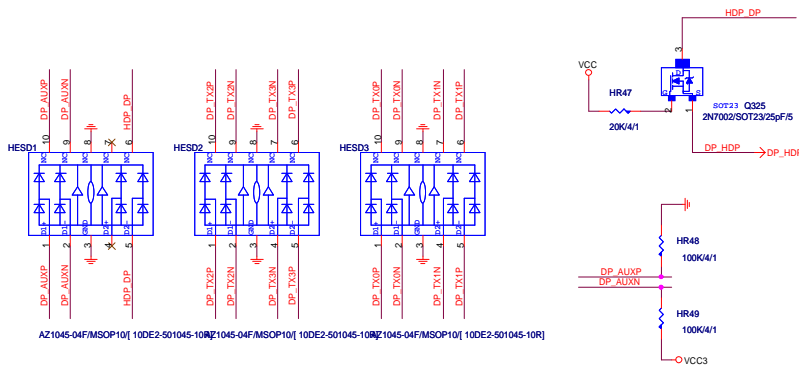
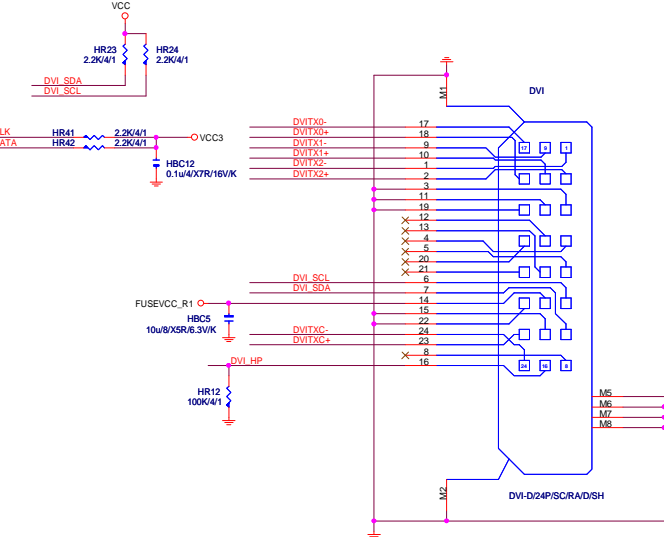
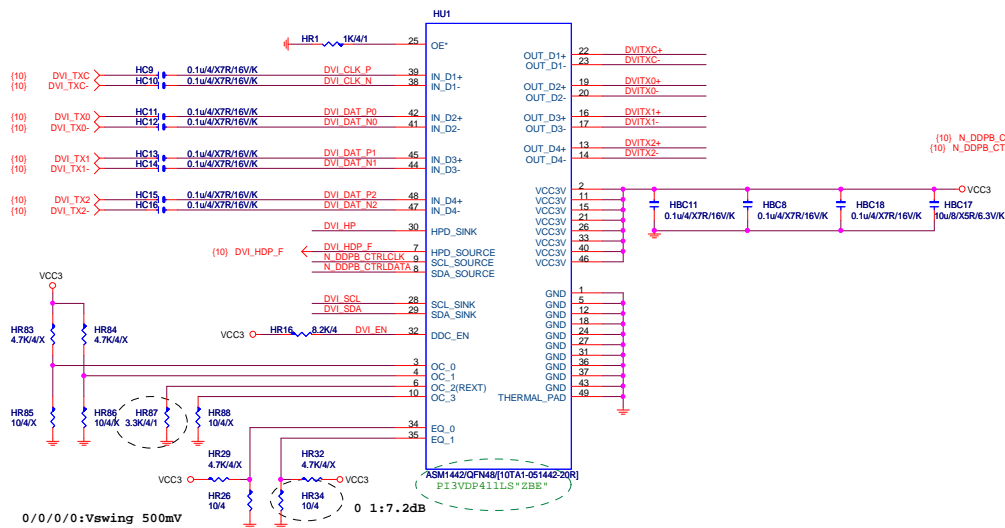
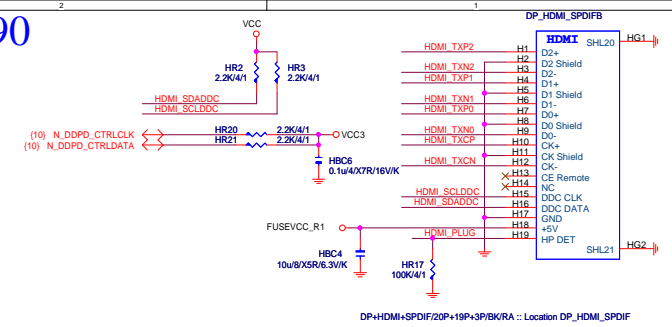
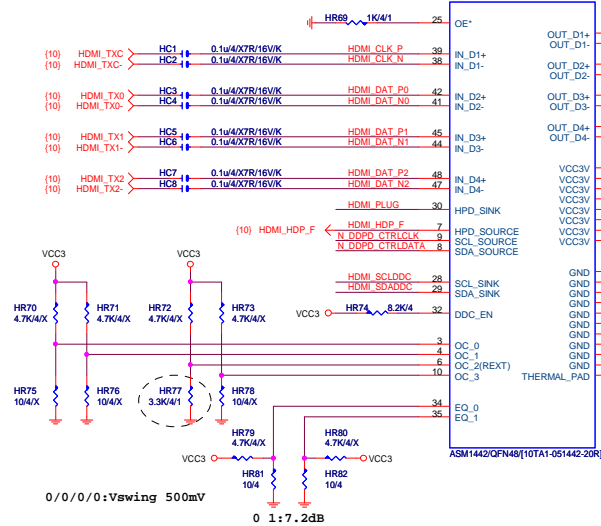


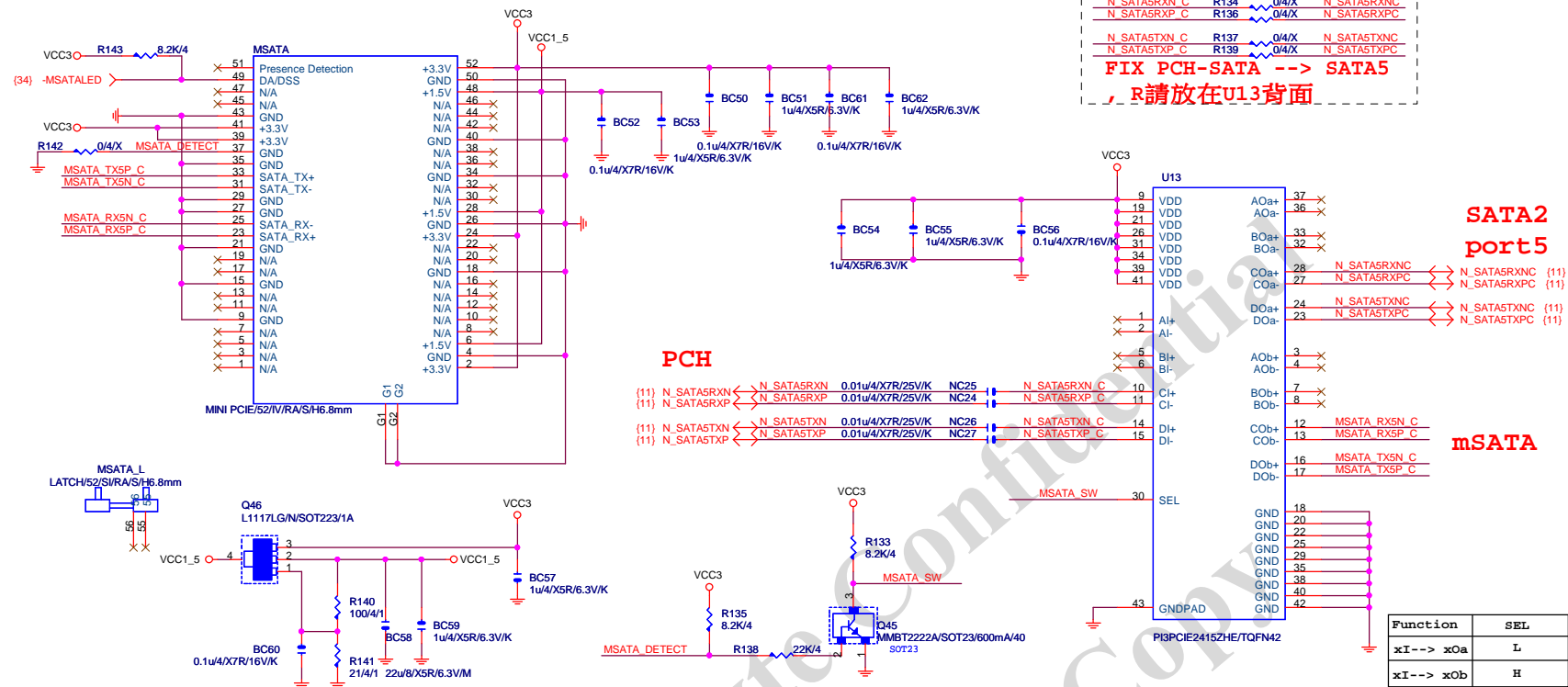
GIGABYTE™

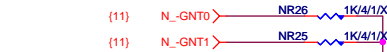
| | | |
|--------|-------------------------|----------------|
| Title | | PCIE_X4 |
| Size | Document Number | GA-Z77X-UD3H |
| Custom | | Rev 1.2 |
| Date: | Thursday, July 25, 2013 | Sheet 18 of 41 |









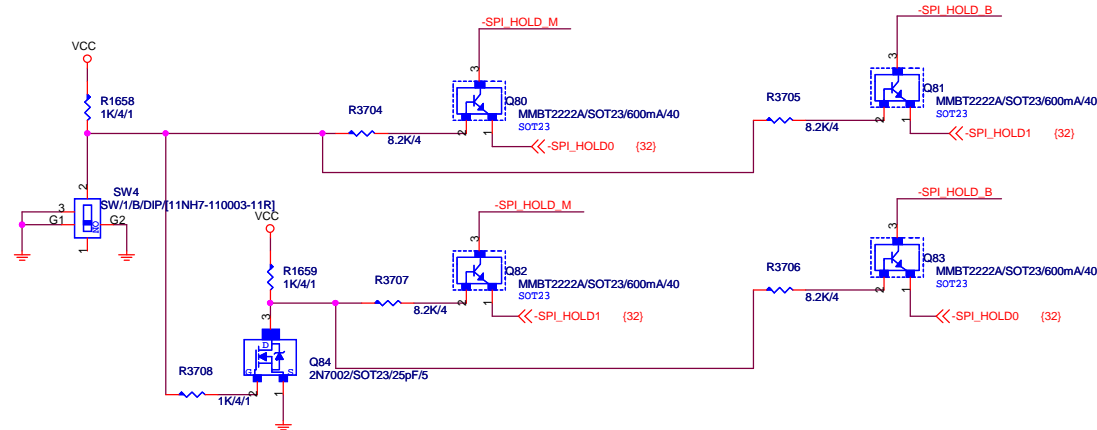
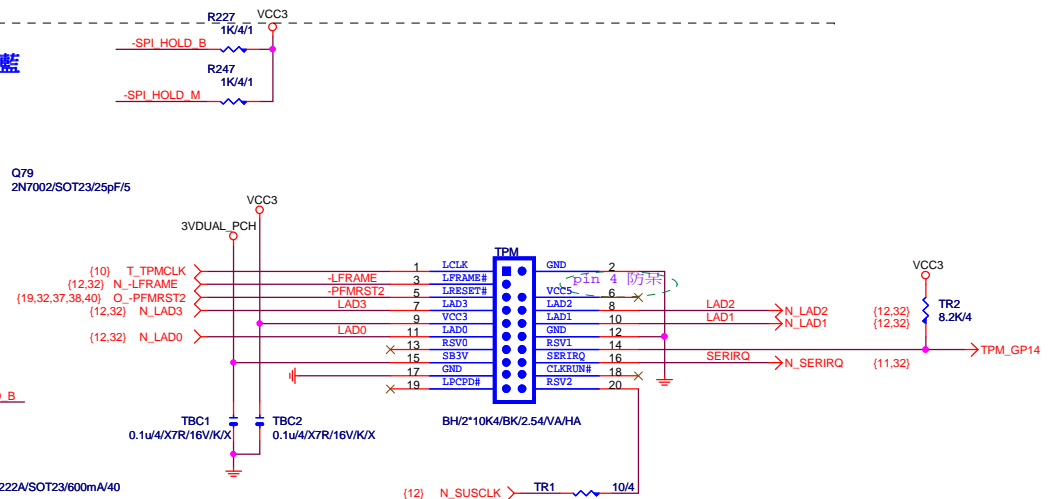
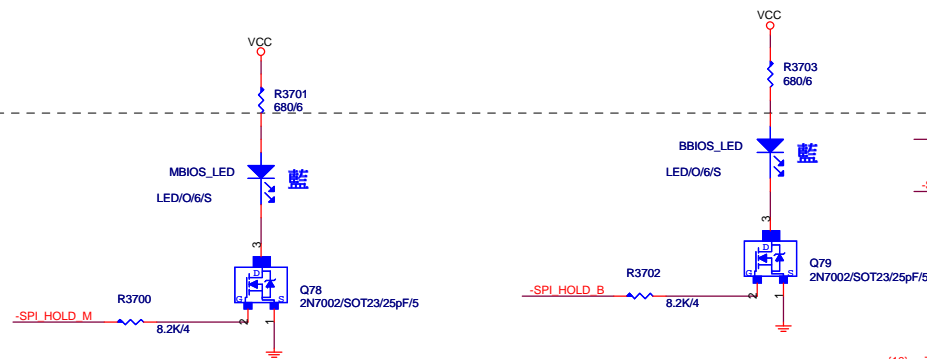
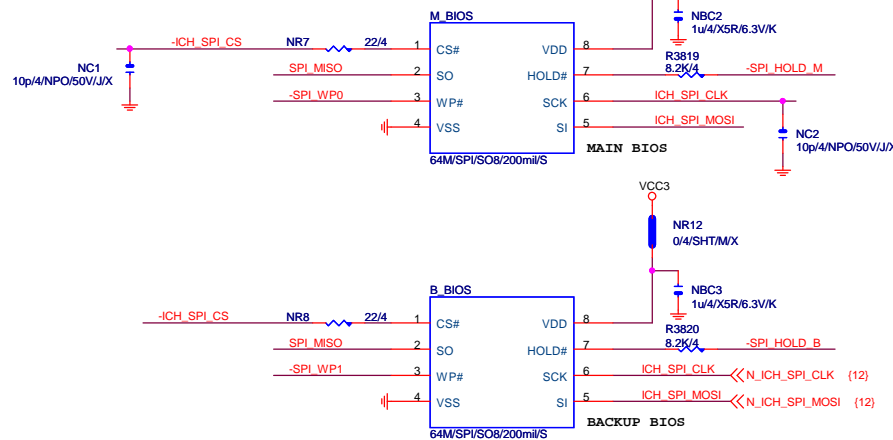


Default int pull up

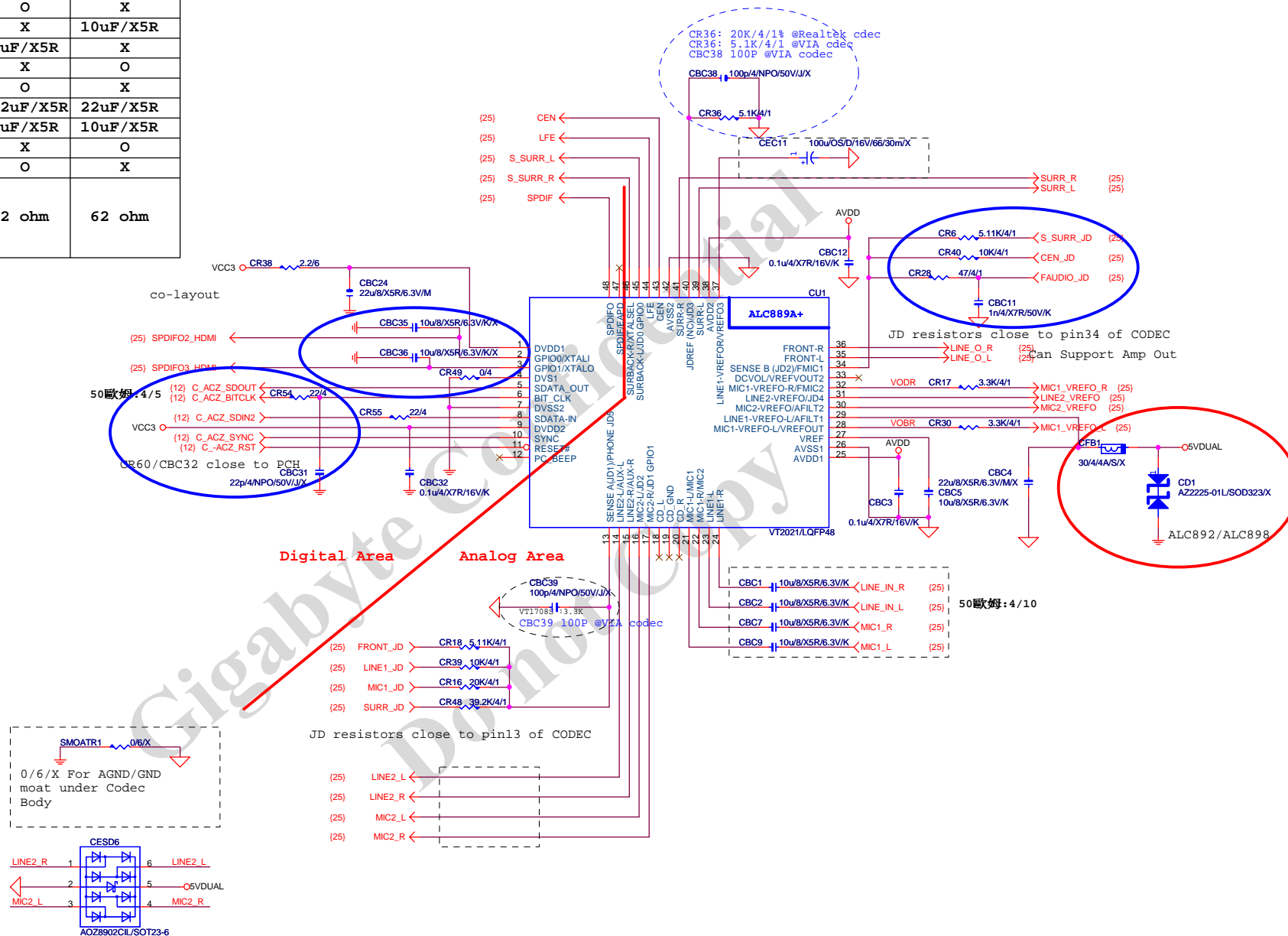


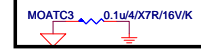
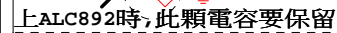
| BOOT DEVICE | GNT0 | GNT1 |
|----------------|------|------|
| LPC | 0 | 0 |
| PCI | 0 | 1 |
| NAND | 1 | 0 |
| SPI | 1 | 1 |

1 means floating
0 means PD 1K

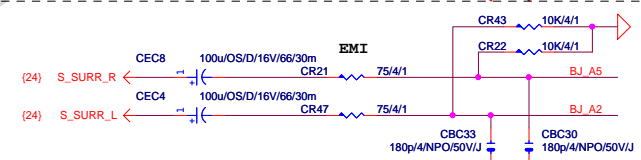


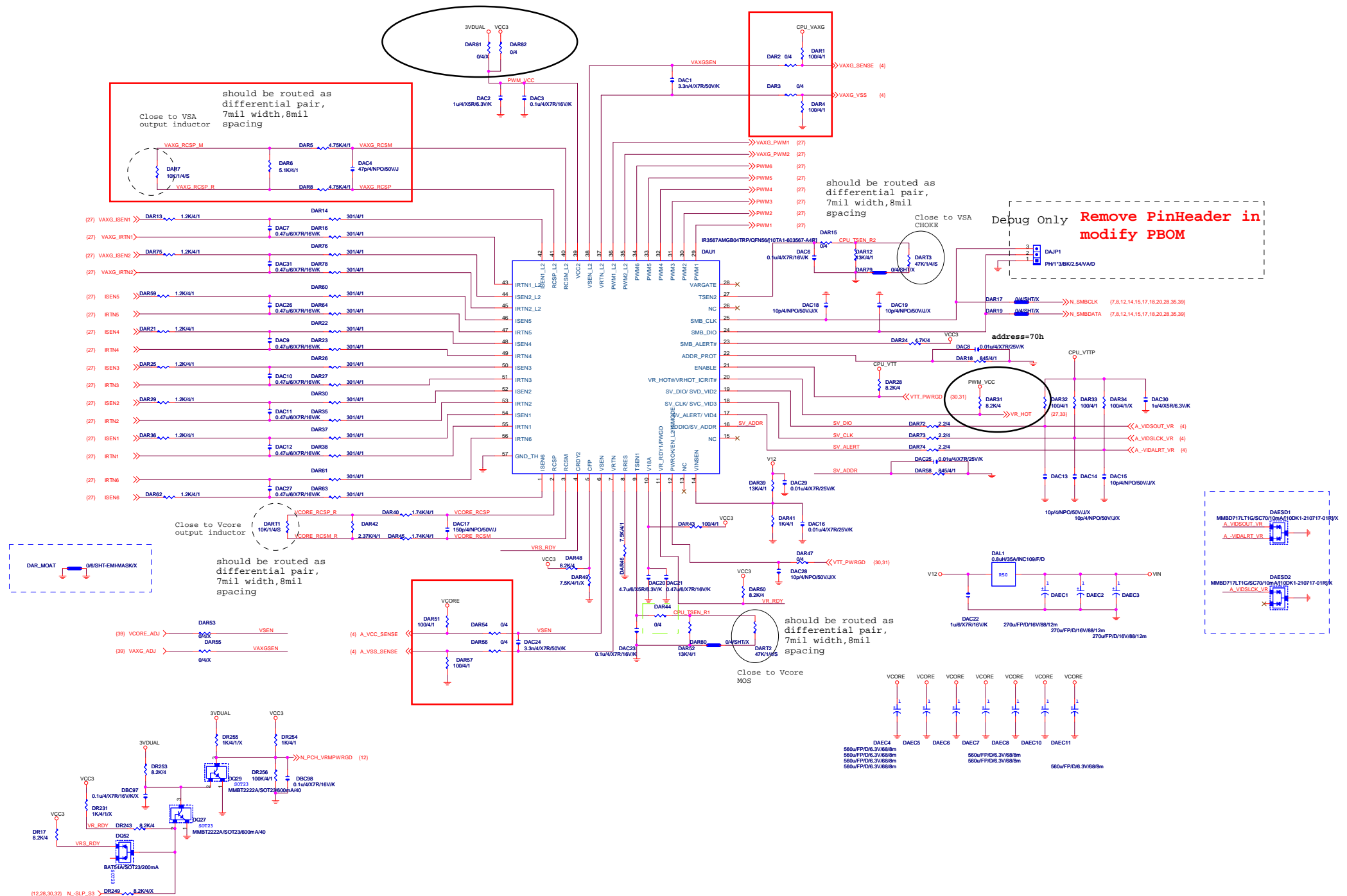
| | ALC889 | ALC889B | ALC898/ALC892 |
|---|----------|----------|---------------|
| CR49 | O | O | X |
| CBC36 | X | X | 10uF/X5R |
| CBC35 | X | 10uF/X5R | X |
| CR52 | O | X | O |
| CR53 | X | O | X |
| CBC1/CBC2 | 22uF/X5R | 22uF/X5R | 22uF/X5R |
| CBC7/CBC9/CBC20/CBC15 | 10uF/X5R | 10uF/X5R | 10uF/X5R |
| CFB1/CD1/CBC4 | X | X | O |
| CD2/CD3/CQ3/CQ4 | O | O | X |
| CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24 | 62 ohm | 62 ohm | 62 ohm |



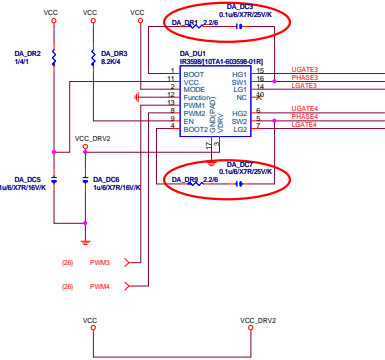


→ F_AUDIO

**AZALIA FRONT PANEL**



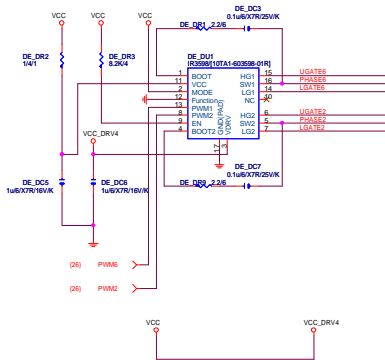
VCORE Phase 3,6



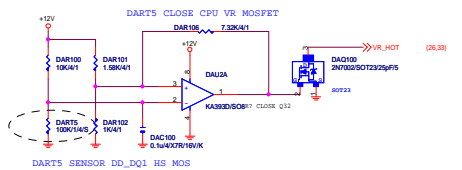
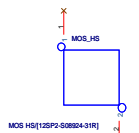
| FUNCTION | MODE | SW MODE | SW MODE | SW MODE |
|----------|------|---------|---------|---------|
| 1 | 1 | 18 | 18 | 18 |
| 2 | 2 | 19 | 19 | 19 |
| 3 | 3 | 20 | 20 | 20 |
| 4 | 4 | 21 | 21 | 21 |
| 5 | 5 | 22 | 22 | 22 |
| 6 | 6 | 23 | 23 | 23 |
| 7 | 7 | 24 | 24 | 24 |
| 8 | 8 | 25 | 25 | 25 |
| 9 | 9 | 26 | 26 | 26 |
| 10 | 10 | 27 | 27 | 27 |
| 11 | 11 | 28 | 28 | 28 |
| 12 | 12 | 29 | 29 | 29 |
| 13 | 13 | 30 | 30 | 30 |
| 14 | 14 | 31 | 31 | 31 |
| 15 | 15 | 32 | 32 | 32 |
| 16 | 16 | 33 | 33 | 33 |
| 17 | 17 | 34 | 34 | 34 |
| 18 | 18 | 35 | 35 | 35 |
| 19 | 19 | 36 | 36 | 36 |
| 20 | 20 | 37 | 37 | 37 |
| 21 | 21 | 38 | 38 | 38 |
| 22 | 22 | 39 | 39 | 39 |
| 23 | 23 | 40 | 40 | 40 |
| 24 | 24 | 41 | 41 | 41 |
| 25 | 25 | 42 | 42 | 42 |
| 26 | 26 | 43 | 43 | 43 |
| 27 | 27 | 44 | 44 | 44 |
| 28 | 28 | 45 | 45 | 45 |
| 29 | 29 | 46 | 46 | 46 |
| 30 | 30 | 47 | 47 | 47 |
| 31 | 31 | 48 | 48 | 48 |
| 32 | 32 | 49 | 49 | 49 |
| 33 | 33 | 50 | 50 | 50 |
| 34 | 34 | 51 | 51 | 51 |
| 35 | 35 | 52 | 52 | 52 |
| 36 | 36 | 53 | 53 | 53 |
| 37 | 37 | 54 | 54 | 54 |
| 38 | 38 | 55 | 55 | 55 |
| 39 | 39 | 56 | 56 | 56 |
| 40 | 40 | 57 | 57 | 57 |
| 41 | 41 | 58 | 58 | 58 |
| 42 | 42 | 59 | 59 | 59 |
| 43 | 43 | 60 | 60 | 60 |
| 44 | 44 | 61 | 61 | 61 |
| 45 | 45 | 62 | 62 | 62 |
| 46 | 46 | 63 | 63 | 63 |
| 47 | 47 | 64 | 64 | 64 |
| 48 | 48 | 65 | 65 | 65 |
| 49 | 49 | 66 | 66 | 66 |
| 50 | 50 | 67 | 67 | 67 |
| 51 | 51 | 68 | 68 | 68 |
| 52 | 52 | 69 | 69 | 69 |
| 53 | 53 | 70 | 70 | 70 |
| 54 | 54 | 71 | 71 | 71 |
| 55 | 55 | 72 | 72 | 72 |
| 56 | 56 | 73 | 73 | 73 |
| 57 | 57 | 74 | 74 | 74 |
| 58 | 58 | 75 | 75 | 75 |
| 59 | 59 | 76 | 76 | 76 |
| 60 | 60 | 77 | 77 | 77 |
| 61 | 61 | 78 | 78 | 78 |
| 62 | 62 | 79 | 79 | 79 |
| 63 | 63 | 80 | 80 | 80 |
| 64 | 64 | 81 | 81 | 81 |
| 65 | 65 | 82 | 82 | 82 |
| 66 | 66 | 83 | 83 | 83 |
| 67 | 67 | 84 | 84 | 84 |
| 68 | 68 | 85 | 85 | 85 |
| 69 | 69 | 86 | 86 | 86 |
| 70 | 70 | 87 | 87 | 87 |
| 71 | 71 | 88 | 88 | 88 |
| 72 | 72 | 89 | 89 | 89 |
| 73 | 73 | 90 | 90 | 90 |
| 74 | 74 | 91 | 91 | 91 |
| 75 | 75 | 92 | 92 | 92 |
| 76 | 76 | 93 | 93 | 93 |
| 77 | 77 | 94 | 94 | 94 |
| 78 | 78 | 95 | 95 | 95 |
| 79 | 79 | 96 | 96 | 96 |
| 80 | 80 | 97 | 97 | 97 |
| 81 | 81 | 98 | 98 | 98 |
| 82 | 82 | 99 | 99 | 99 |
| 83 | 83 | 100 | 100 | 100 |

In Quad mode, I2C pin1 link to I2C pin10
I2C pin10 link to I2C pin1 without P0

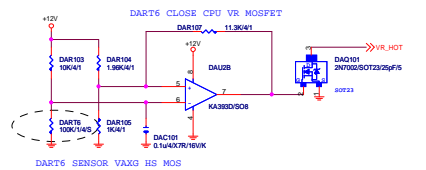
VCORE Phase 5,2



MOS HEATSINK

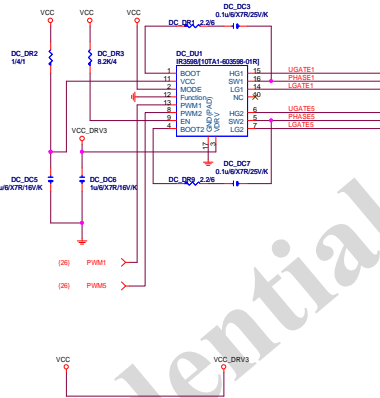


DART5 SENSOR DD_Q1 HS MOS



DART6 SENSOR VAXG HS MOS

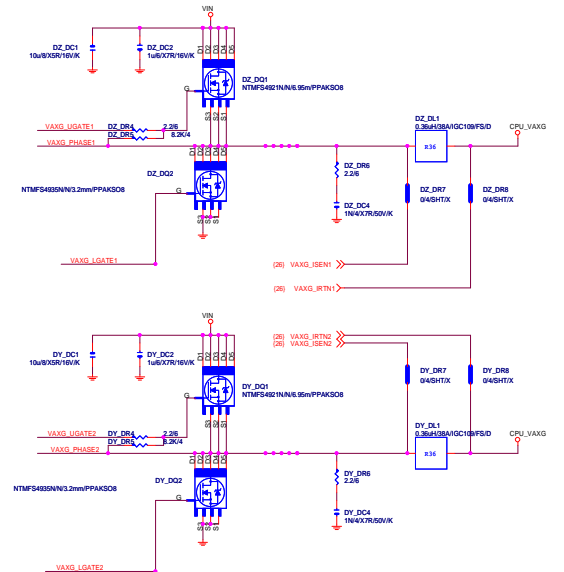
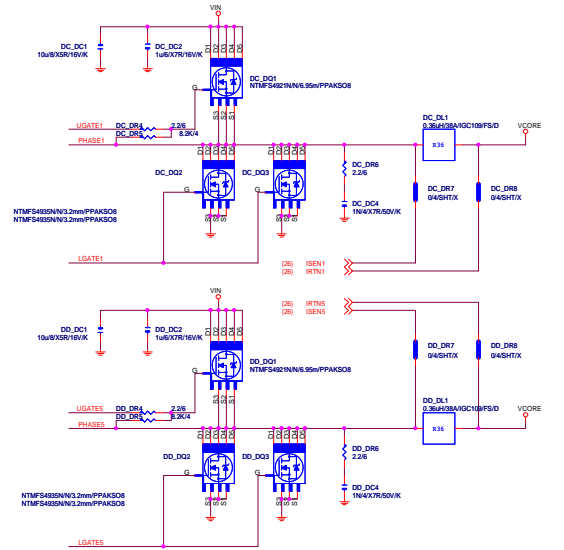
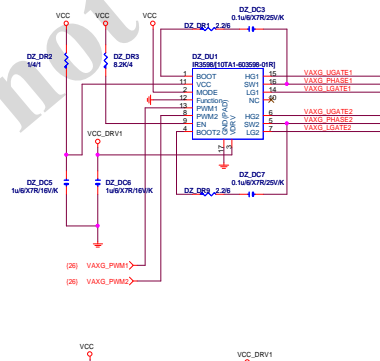
VCORE Phase 1,4

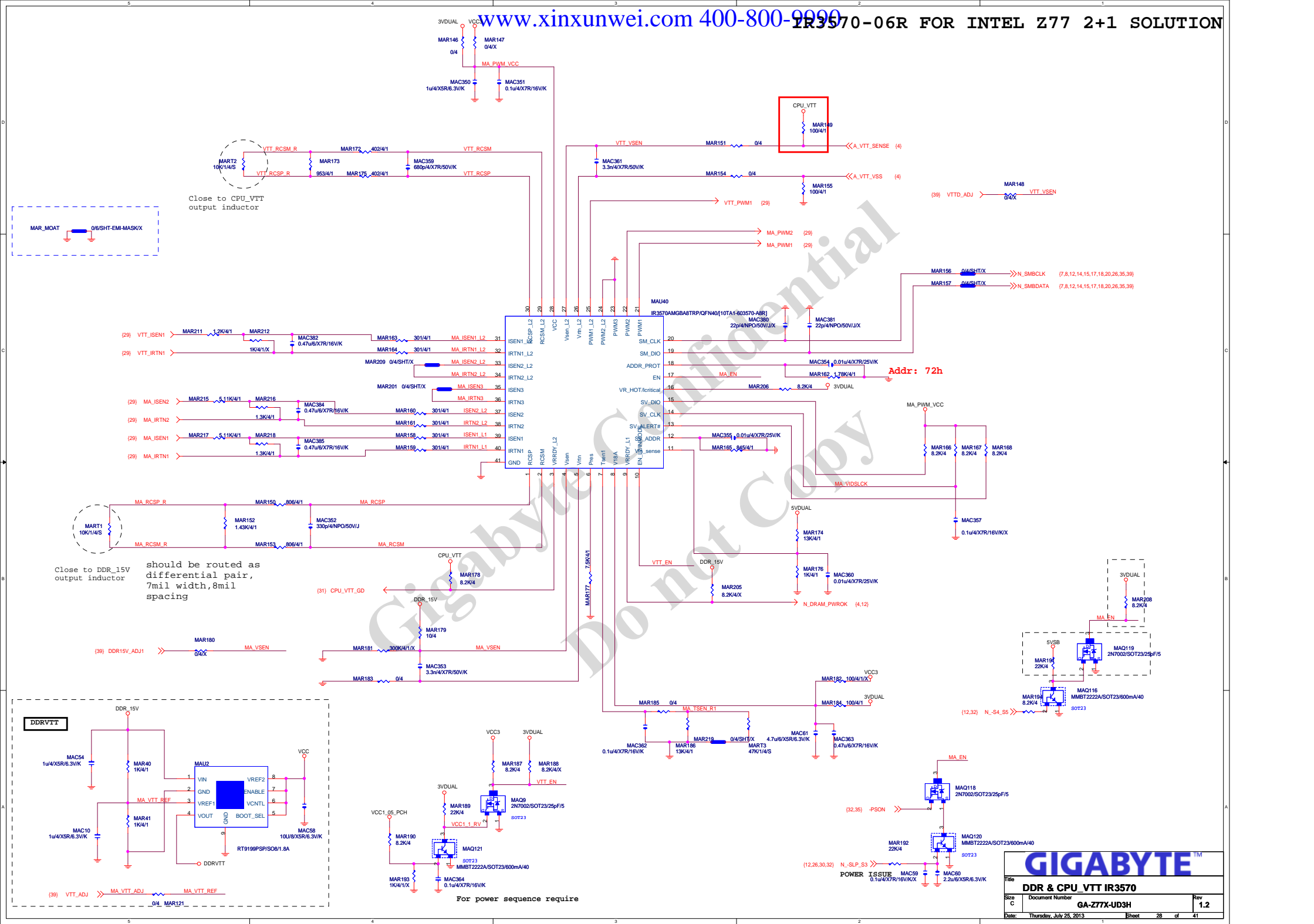


| FUNCTION | MODE | SW MODE | SW MODE | SW MODE |
|----------|------|---------|---------|---------|
| 1 | 1 | 18 | 18 | 18 |
| 2 | 2 | 19 | 19 | 19 |
| 3 | 3 | 20 | 20 | 20 |
| 4 | 4 | 21 | 21 | 21 |
| 5 | 5 | 22 | 22 | 22 |
| 6 | 6 | 23 | 23 | 23 |
| 7 | 7 | 24 | 24 | 24 |
| 8 | 8 | 25 | 25 | 25 |
| 9 | 9 | 26 | 26 | 26 |
| 10 | 10 | 27 | 27 | 27 |
| 11 | 11 | 28 | 28 | 28 |
| 12 | 12 | 29 | 29 | 29 |
| 13 | 13 | 30 | 30 | 30 |
| 14 | 14 | 31 | 31 | 31 |
| 15 | 15 | 32 | 32 | 32 |
| 16 | 16 | 33 | 33 | 33 |
| 17 | 17 | 34 | 34 | 34 |
| 18 | 18 | 35 | 35 | 35 |
| 19 | 19 | 36 | 36 | 36 |
| 20 | 20 | 37 | 37 | 37 |
| 21 | 21 | 38 | 38 | 38 |
| 22 | 22 | 39 | 39 | 39 |
| 23 | 23 | 40 | 40 | 40 |
| 24 | 24 | 41 | 41 | 41 |
| 25 | 25 | 42 | 42 | 42 |
| 26 | 26 | 43 | 43 | 43 |
| 27 | 27 | 44 | 44 | 44 |
| 28 | 28 | 45 | 45 | 45 |
| 29 | 29 | 46 | 46 | 46 |
| 30 | 30 | 47 | 47 | 47 |
| 31 | 31 | 48 | 48 | 48 |
| 32 | 32 | 49 | 49 | 49 |
| 33 | 33 | 50 | 50 | 50 |
| 34 | 34 | 51 | 51 | 51 |
| 35 | 35 | 52 | 52 | 52 |
| 36 | 36 | 53 | 53 | 53 |
| 37 | 37 | 54 | 54 | 54 |
| 38 | 38 | 55 | 55 | 55 |
| 39 | 39 | 56 | 56 | 56 |
| 40 | 40 | 57 | 57 | 57 |
| 41 | 41 | 58 | 58 | 58 |
| 42 | 42 | 59 | 59 | 59 |
| 43 | 43 | 60 | 60 | 60 |
| 44 | 44 | 61 | 61 | 61 |
| 45 | 45 | 62 | 62 | 62 |
| 46 | 46 | 63 | 63 | 63 |
| 47 | 47 | 64 | 64 | 64 |
| 48 | 48 | 65 | 65 | 65 |
| 49 | 49 | 66 | 66 | 66 |
| 50 | 50 | 67 | 67 | 67 |
| 51 | 51 | 68 | 68 | 68 |
| 52 | 52 | 69 | 69 | 69 |
| 53 | 53 | 70 | 70 | 70 |
| 54 | 54 | 71 | 71 | 71 |
| 55 | 55 | 72 | 72 | 72 |
| 56 | 56 | 73 | 73 | 73 |
| 57 | 57 | 74 | 74 | 74 |
| 58 | 58 | 75 | 75 | 75 |
| 59 | 59 | 76 | 76 | 76 |
| 60 | 60 | 77 | 77 | 77 |
| 61 | 61 | 78 | 78 | 78 |
| 62 | 62 | 79 | 79 | 79 |
| 63 | 63 | 80 | 80 | 80 |
| 64 | 64 | 81 | 81 | 81 |
| 65 | 65 | 82 | 82 | 82 |
| 66 | 66 | 83 | 83 | 83 |
| 67 | 67 | 84 | 84 | 84 |
| 68 | 68 | 85 | 85 | 85 |
| 69 | 69 | 86 | 86 | 86 |
| 70 | 70 | 87 | 87 | 87 |
| 71 | 71 | 88 | 88 | 88 |
| 72 | 72 | 89 | 89 | 89 |
| 73 | 73 | 90 | 90 | 90 |
| 74 | 74 | 91 | 91 | 91 |
| 75 | 75 | 92 | 92 | 92 |
| 76 | 76 | 93 | 93 | 93 |
| 77 | 77 | 94 | 94 | 94 |
| 78 | 78 | 95 | 95 | 95 |
| 79 | 79 | 96 | 96 | 96 |
| 80 | 80 | 97 | 97 | 97 |
| 81 | 81 | 98 | 98 | 98 |
| 82 | 82 | 99 | 99 | 99 |
| 83 | 83 | 100 | 100 | 100 |

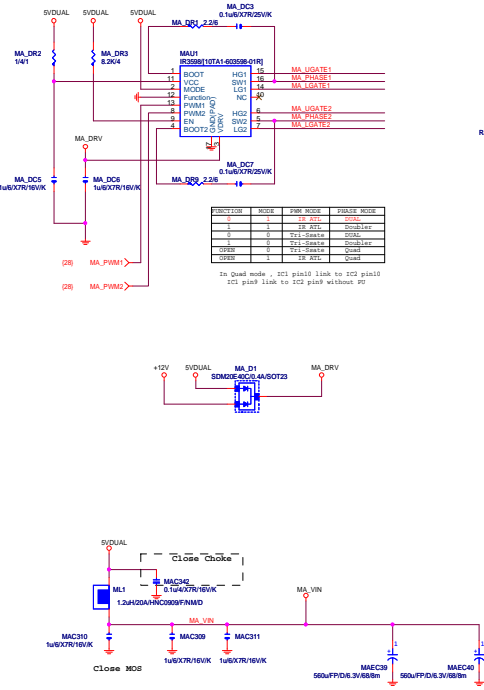
In Quad mode, I2C pin1 link to I2C pin10
I2C pin10 link to I2C pin1 without P0

VAXG Phase

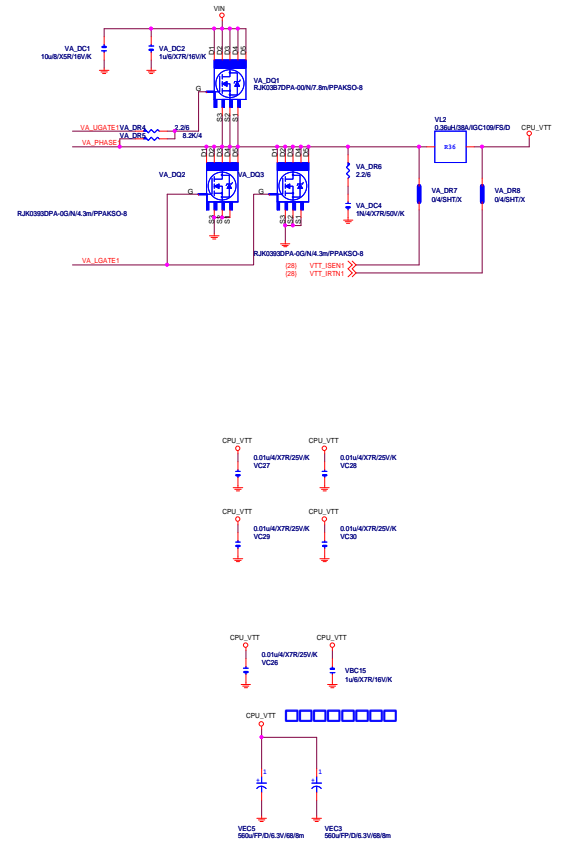
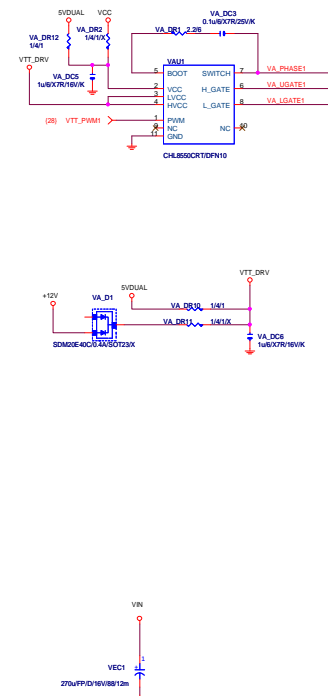


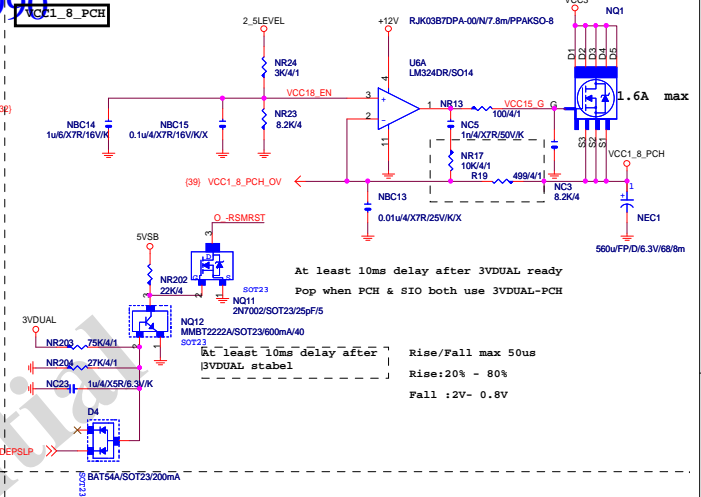
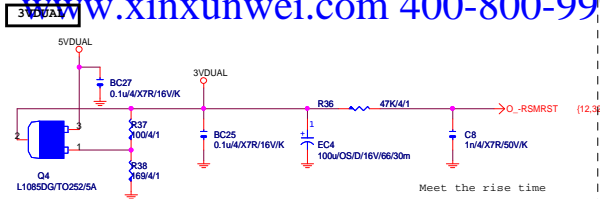
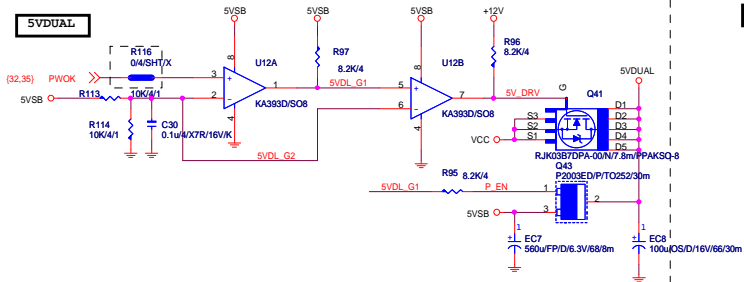


DDR_15V

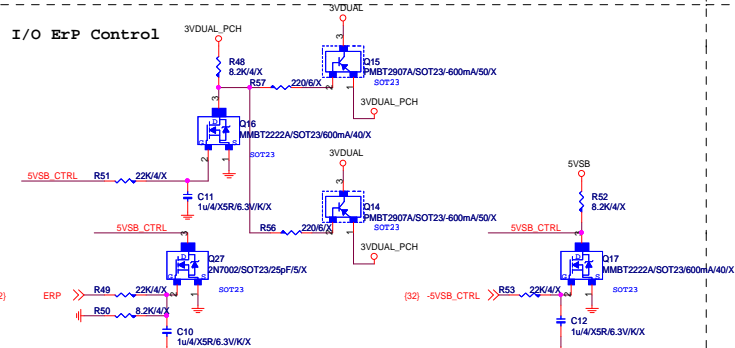


CPU_VTT

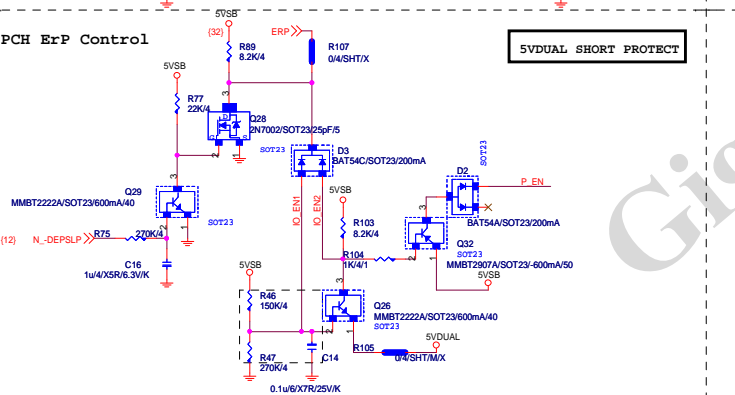




I/O ErP Control

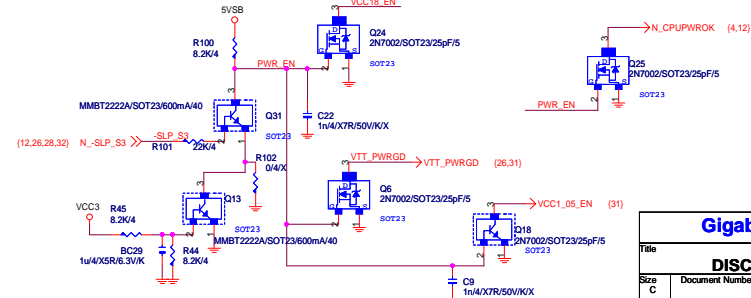
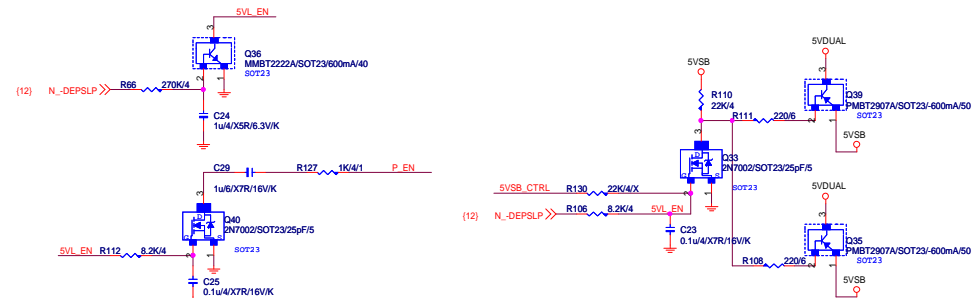
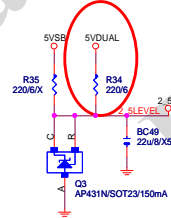


PCH ErP Control



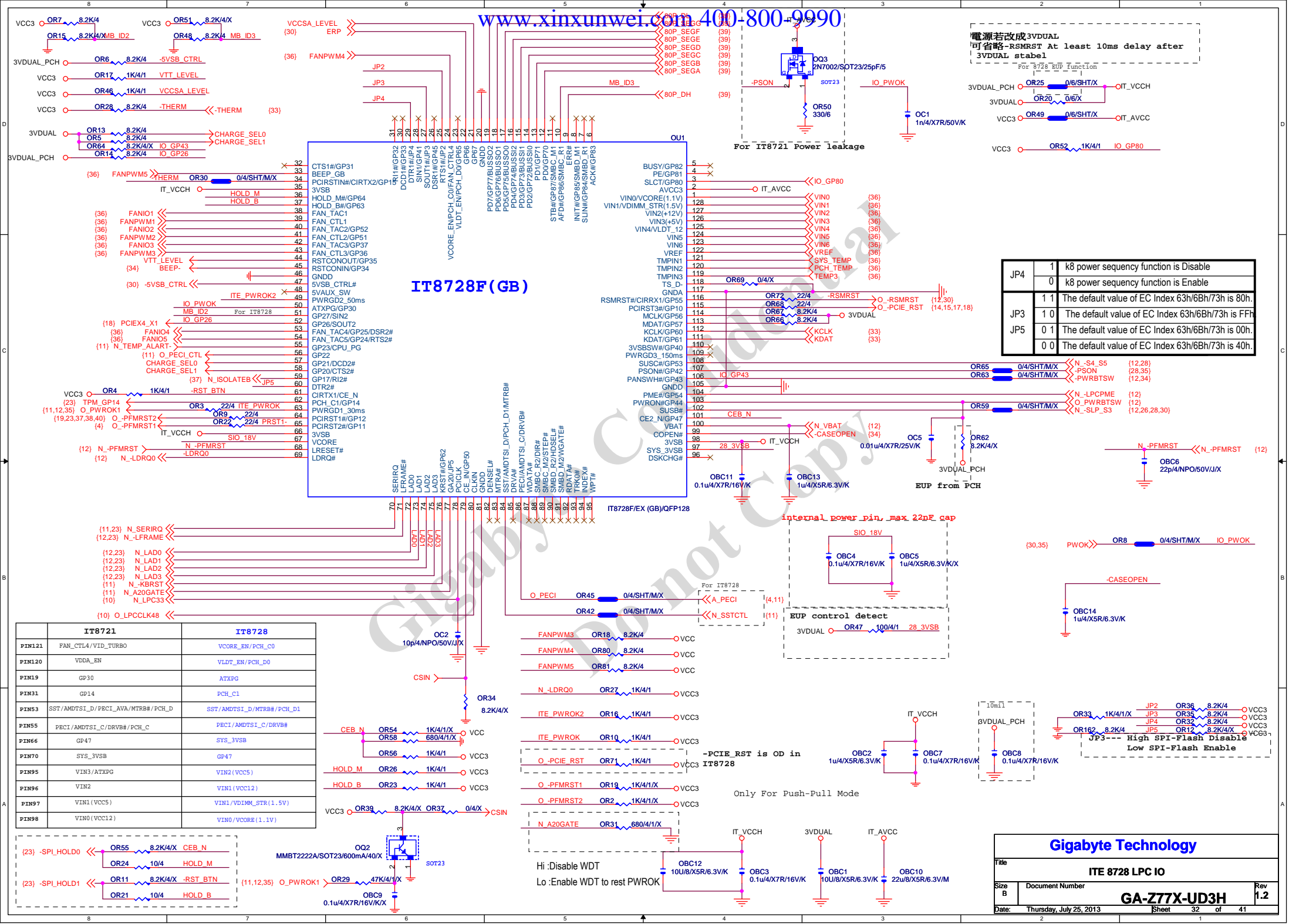
5VDUAL SHORT PROTECT

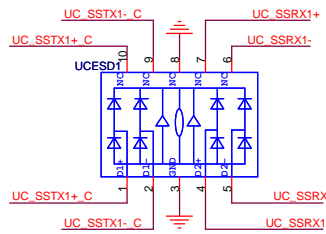
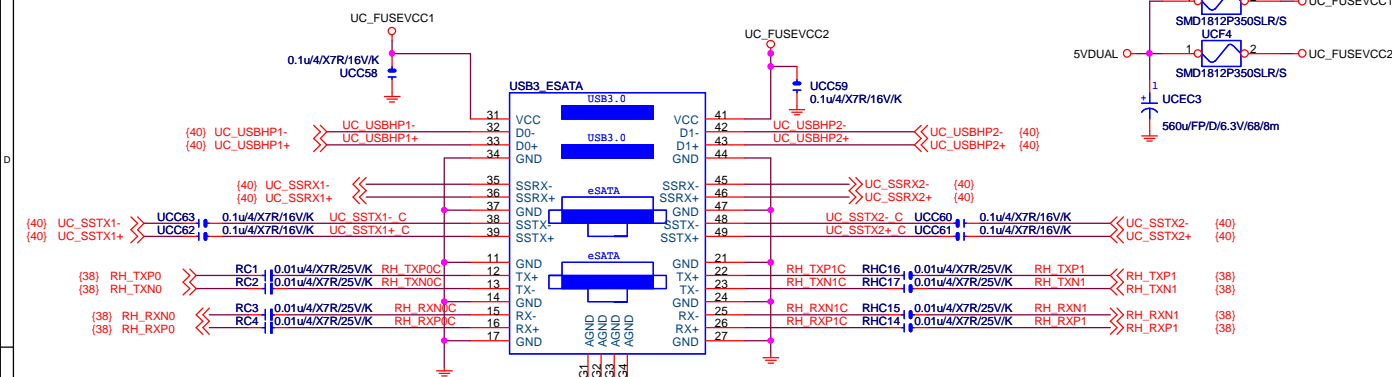
ErP



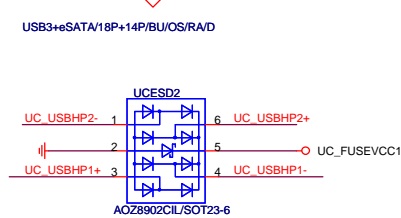
Gigabyte Technology

| Title | | |
|----------------|-------------------------|----------------|
| DISCRETE POWER | | |
| Size C | Document Number | GA-Z77X-UD3H |
| Date | Thursday, July 25, 2013 | Sheet 30 of 41 |

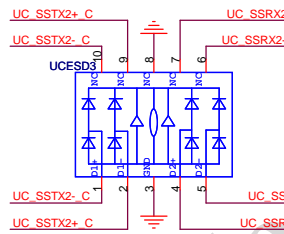




Close to connector

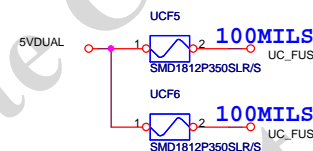
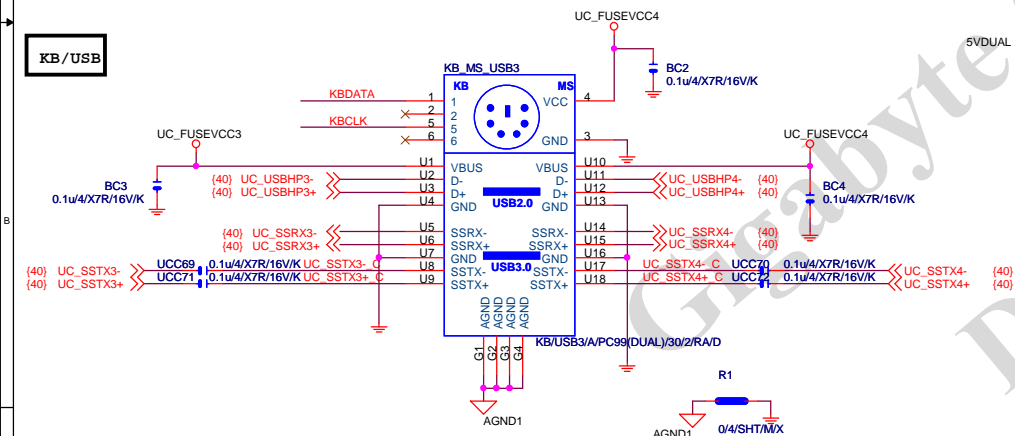


Close to connector



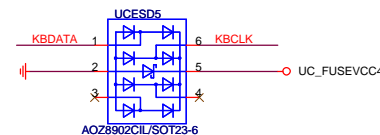
Close to connector

KB / USB

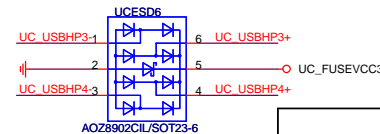


100MILS

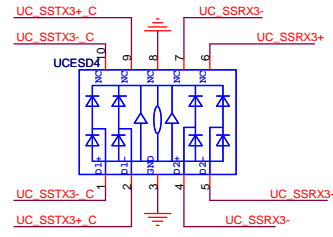
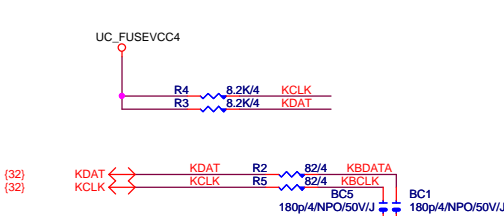
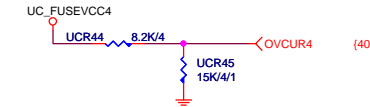
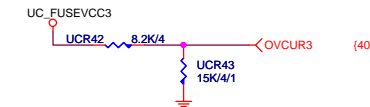
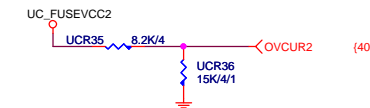
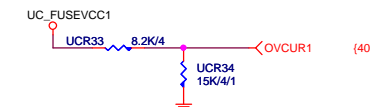
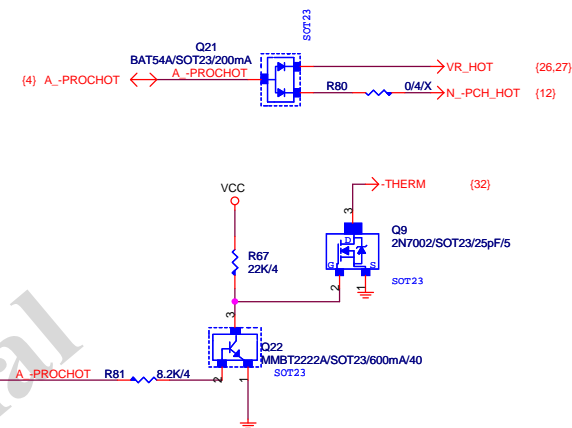
100MILS



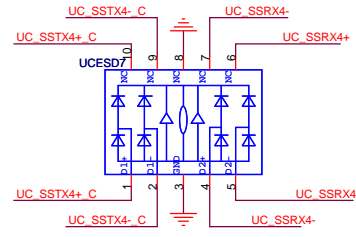
Close to connector



Close to connector

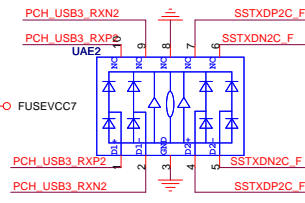
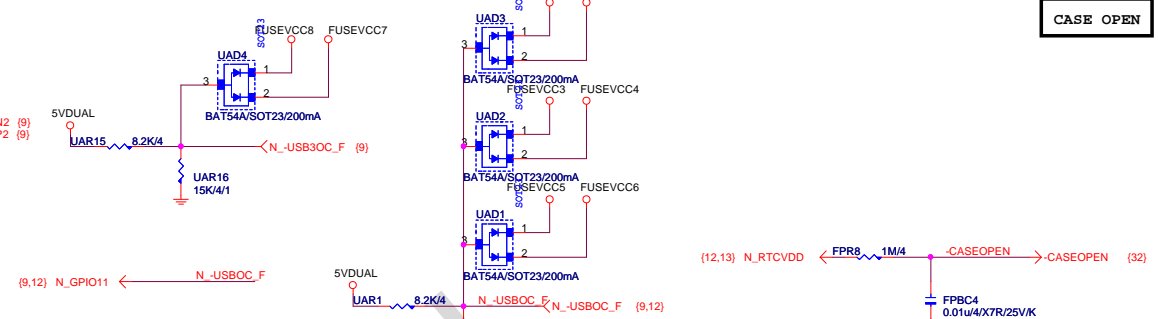


Close to connector

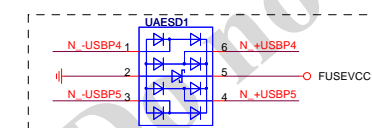
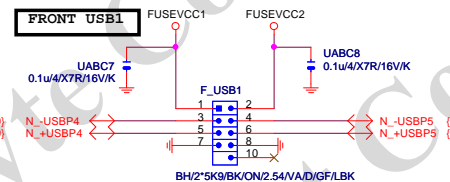
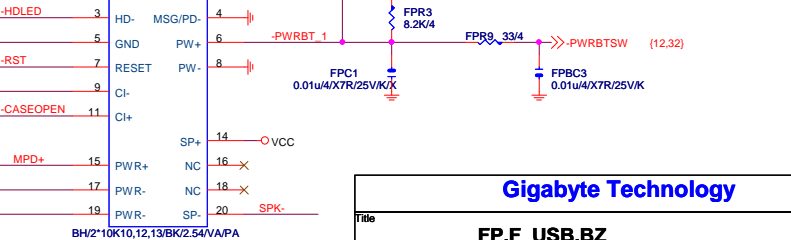
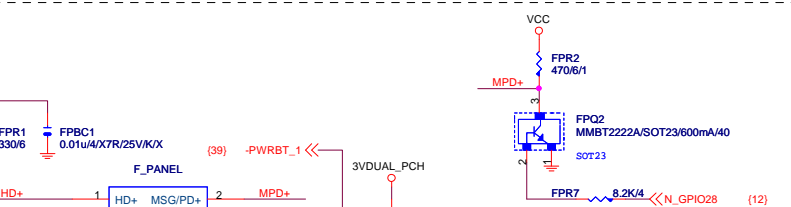
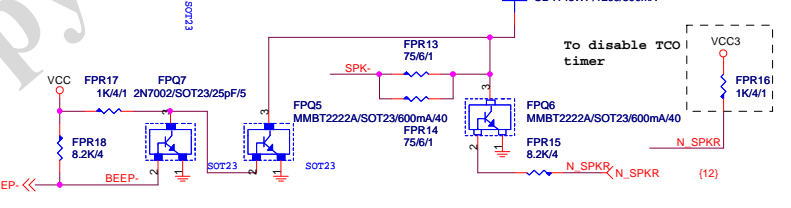
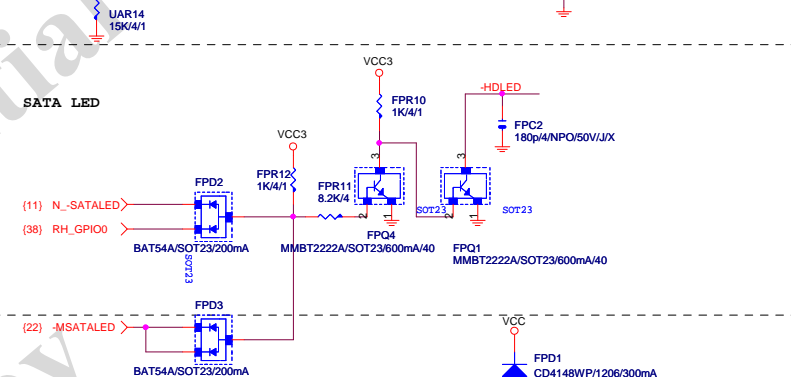
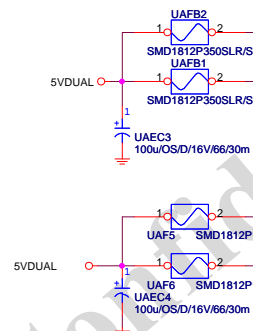


Close to connector

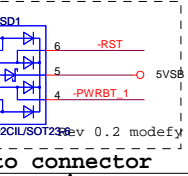
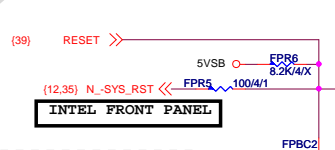
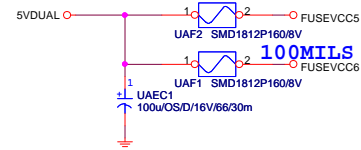
| Gigabyte Technology | | | |
|----------------------|-------------------------|-------|----------|
| File | | | |
| USB3_ESATA / KB_USB3 | | | |
| Size | Document Number | Rev | |
| Custom | GA-Z77X-UD3H | 1.2 | |
| Date: | Thursday, July 25, 2013 | Sheet | 33 of 41 |



Close to connector



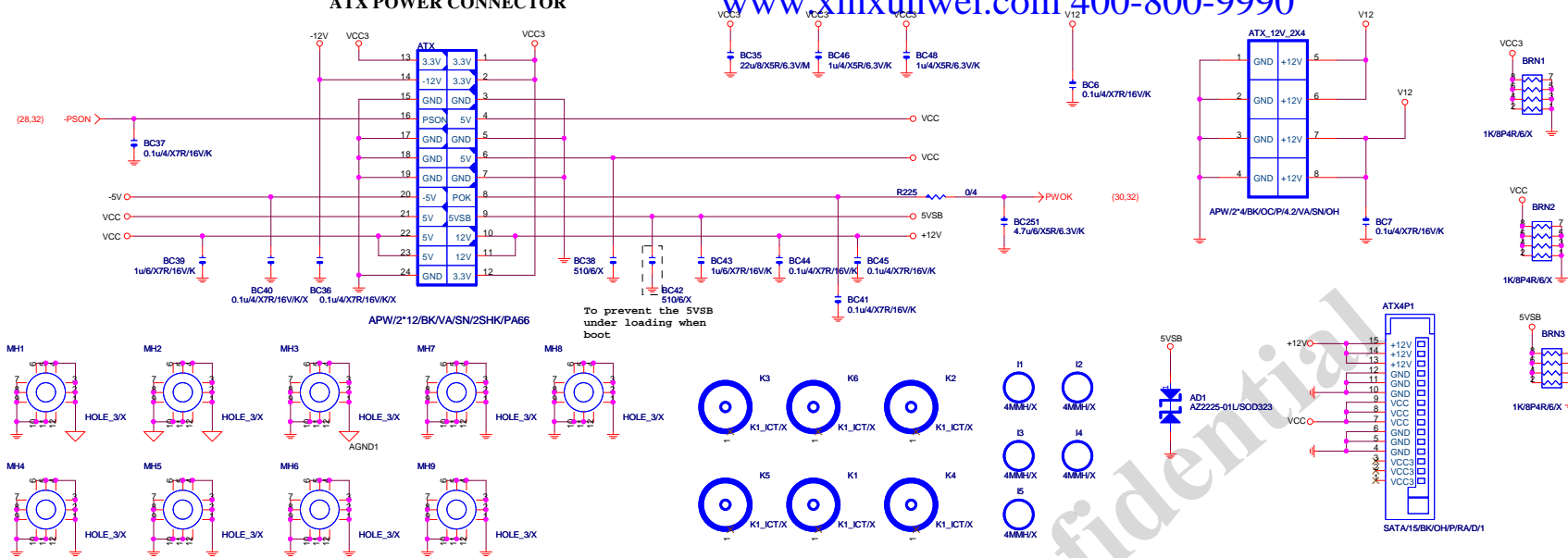
Close to connector



Close to connector

ATX POWER CONNECTOR

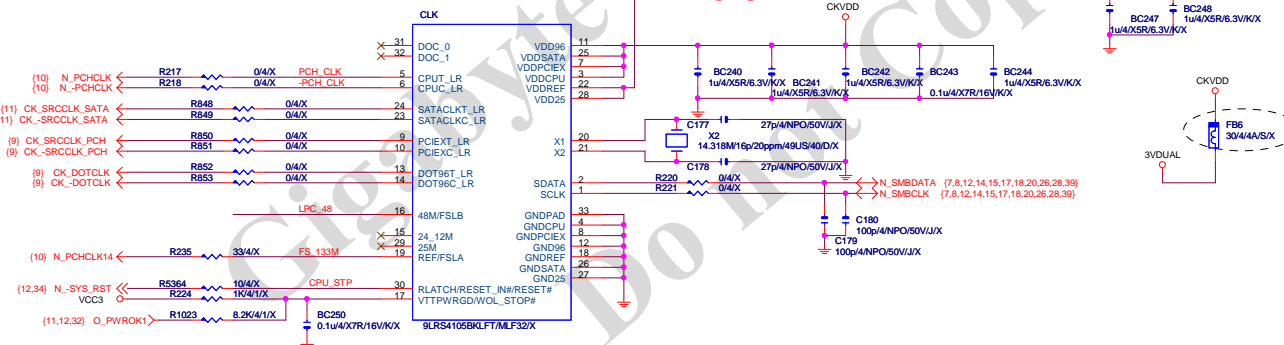
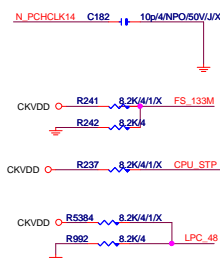
www.xinxunwei.com 400-800-9990



CLK GEN CK505

CPU Frequency Selection

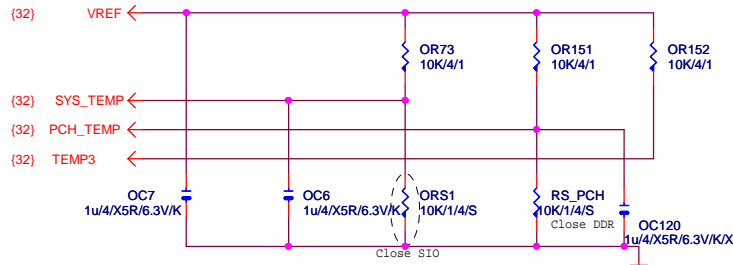
| FSLB | FSLA | CPU |
|------|------|----------------|
| 0 | 0 | 100M <Default> |
| 0 | 1 | 133M |
| 1 | 0 | 200M |
| 1 | 1 | 166M |



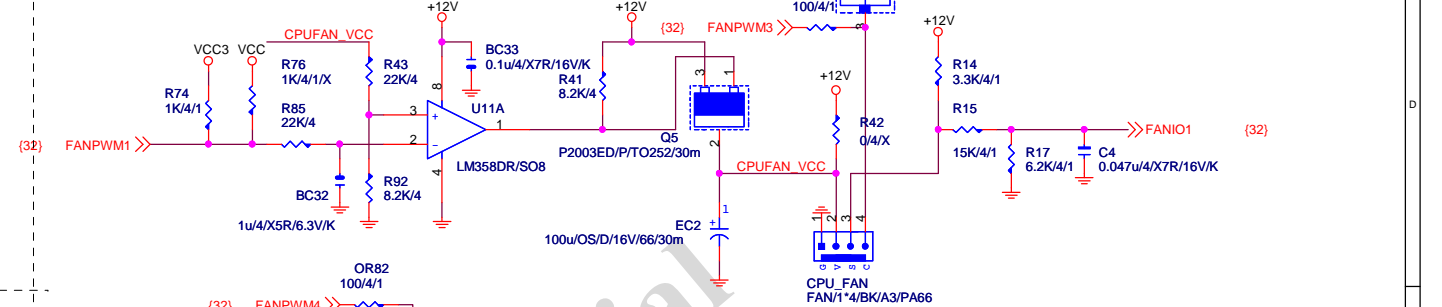
Gigabyte Technology

| | | |
|--------|-------------------------|---------------------|
| Title | | ATX POWER CONNECTOR |
| Size | | GA-Z77X-UD3H |
| Custom | Document Number | Rev 1.2 |
| Date: | Thursday, July 25, 2013 | Sheet 35 of 41 |

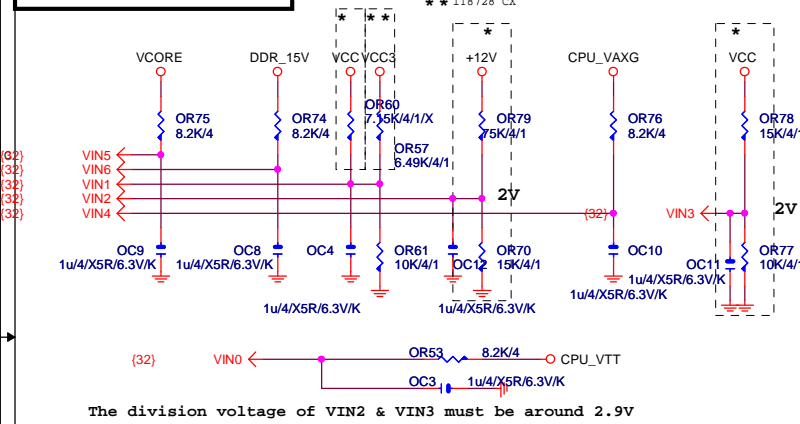
TEMP H/W MONITOR



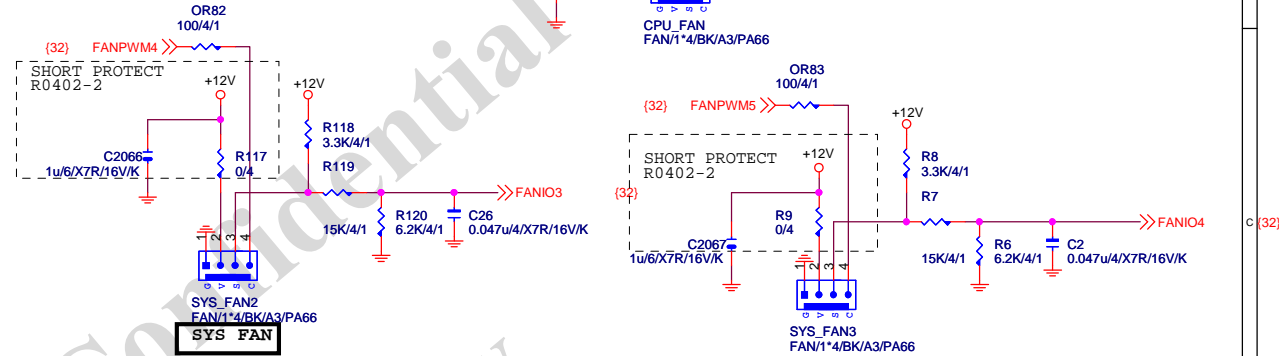
CPU SMART FAN



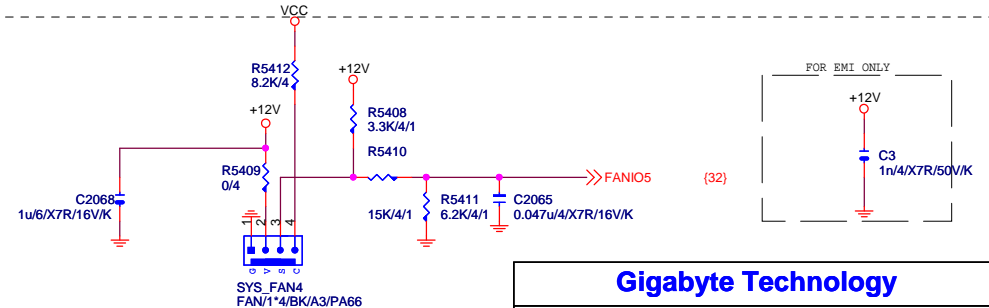
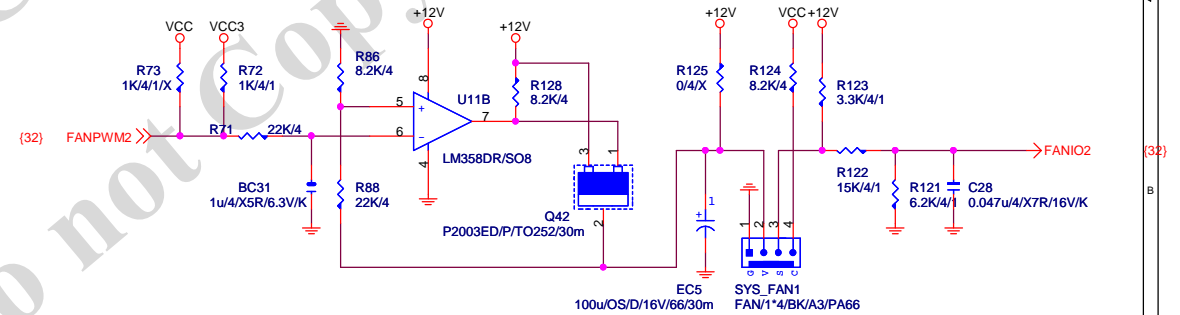
VOLTAGE-- H/W MONITOR



SYS FAN

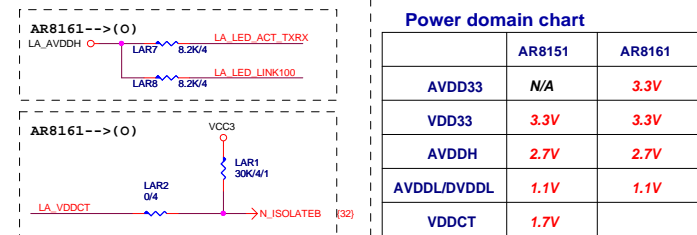
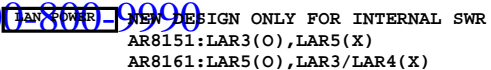


Linear SYS_FAN



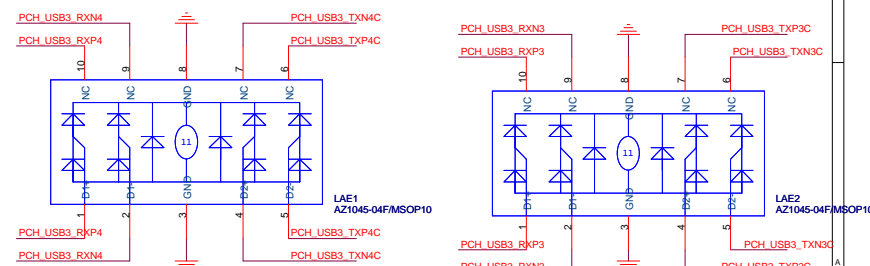
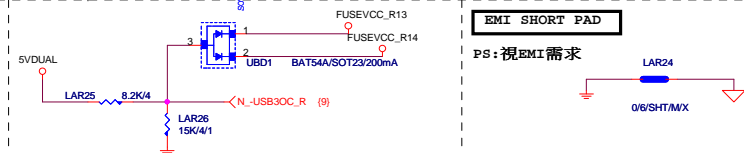
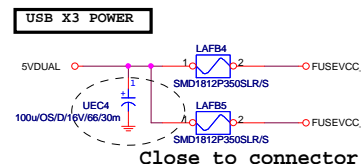
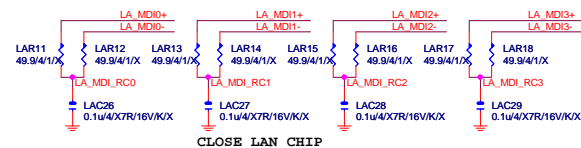
Gigabyte Technology

| Title | | | |
|---------------------|-------------------------|-------|----------|
| HWM,KB/MS, FAN CTRL | | | |
| Size | Document Number | Rev | |
| Custom | GA-Z77X-UD3H | 1.2 | |
| Date: | Thursday, July 25, 2013 | Sheet | 36 of 41 |

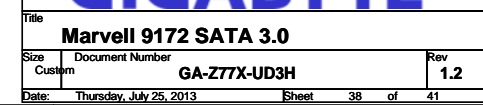


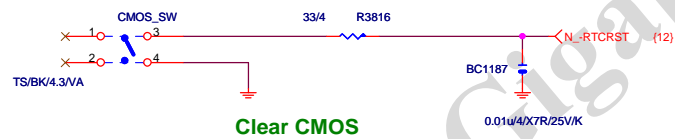
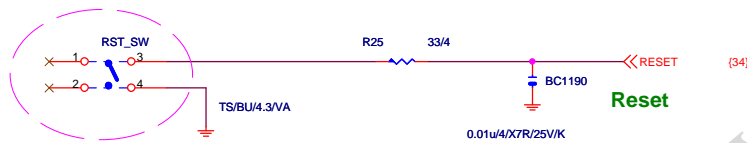
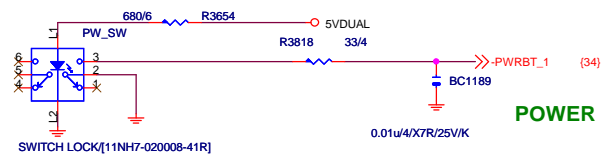
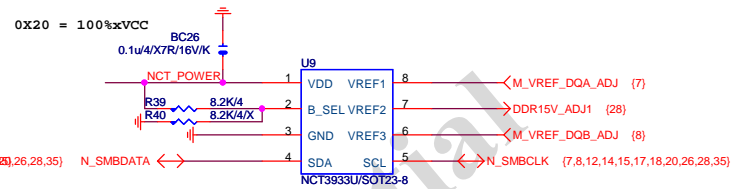
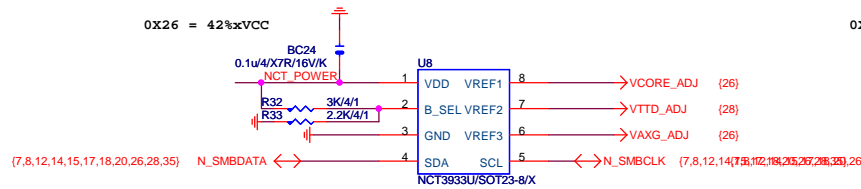
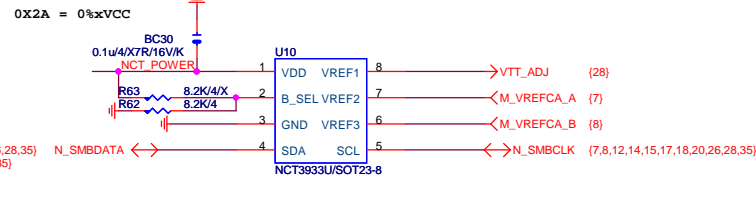
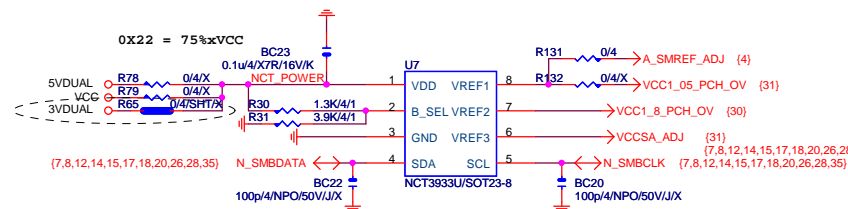
| | AR8151 | AR8161 |
|--------------------|---------------|---------------|
| AVDD33 | N/A | 3.3V |
| VDD33 | 3.3V | 3.3V |
| AVDDH | 2.7V | 2.7V |
| AVDDL/DVDDL | 1.1V | 1.1V |
| VDDCT | 1.7V | |

MDI : AR8161-->N/A

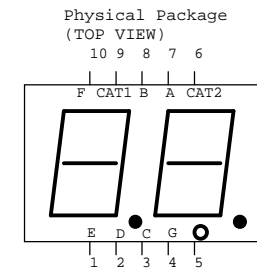
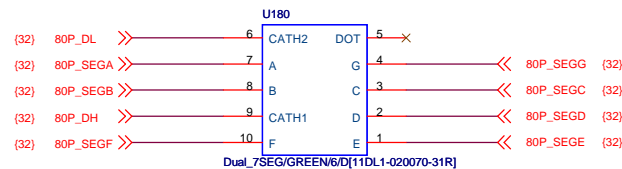
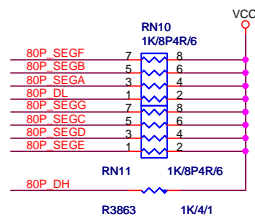


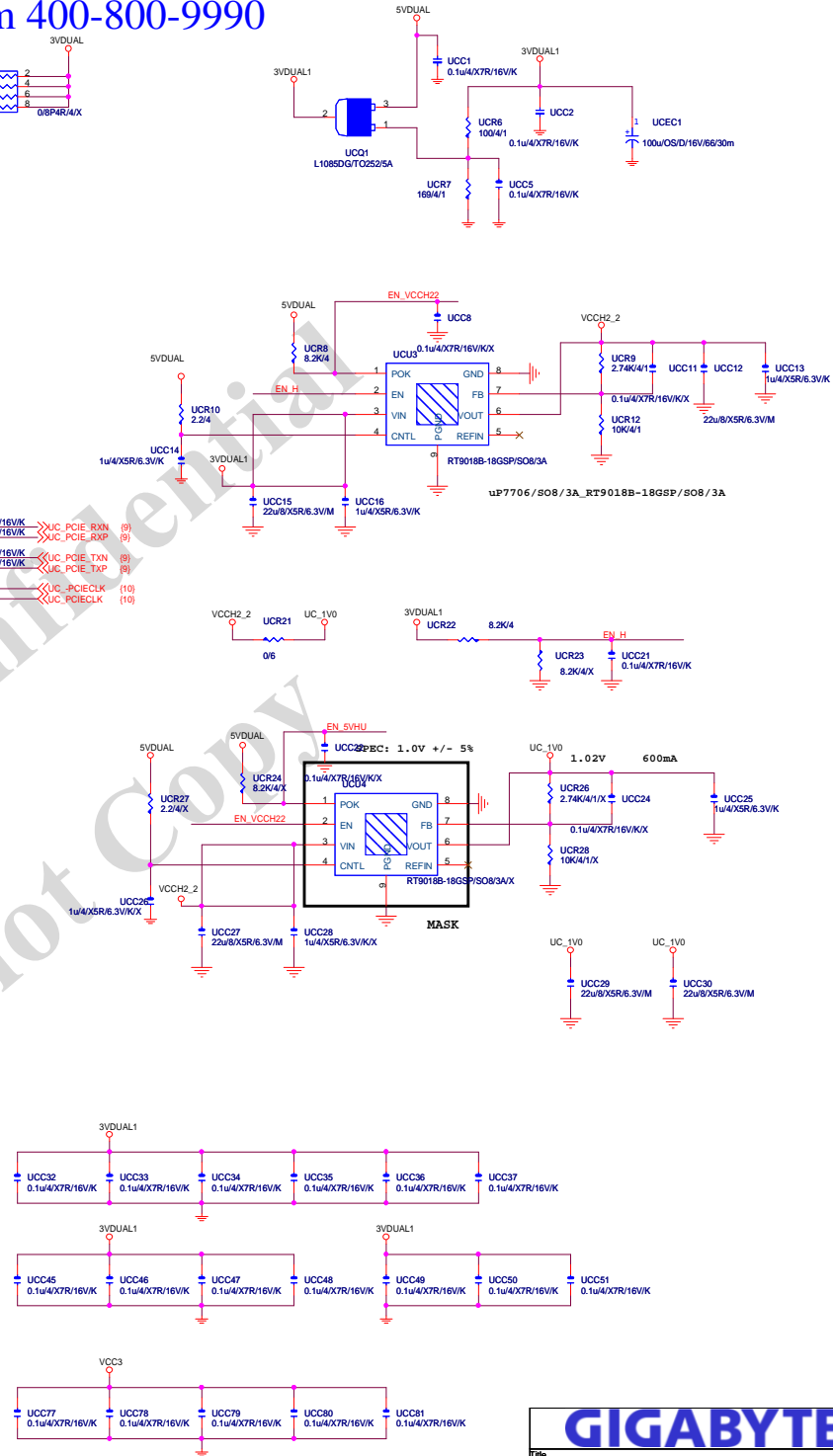
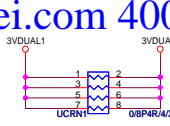
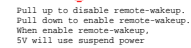
注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]





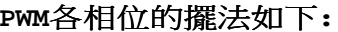
80 PORT





Super I/O ITE8720 GPIO table

| PIN NAME | USAGE | NOTE |
|----------------------------|-------------------|------------------|
| FAN_TAC2/GP52 | FANIO2 | |
| FAN_TAC3/GP37 | FANIO3 | |
| VIDO3/FAN_TAC4/GP25/DSR2# | FANIO4 | |
| FAN_CTL2/GP51 | FANPWM2 | |
| FAN_CTL3/GP36 | FANPWM3 | |
| VID4/GP34 | BEEP- | |
| VID3/GP33 | TURBO1 | |
| VID2/GP32 | TURBO0 | |
| VCORE_GOOD/VID6/GP63 | CPUT_LED1_C | |
| VID5/GP35 | CPUT_LED2_C | |
| VID1/GP31 | CPUT_LED3_C | |
| VID0/GP30 | -LAN1_DSM | NBT_LED1_C |
| SLCT/GP80 | CPU_LED1_C | |
| PE/GP81 | CPU_LED2_C | |
| BUSY/GP82 | CPU_LED3_C | |
| PD3/GP73/BUSS11 | SB_LED1_C | |
| PD4/GP74/BUSS12 | SB_LED2_C | |
| VCORE_EN/VID7/GP64 | IT_GP64 | SB_LED3_C |
| PD0/GP70 | NB_LED1_C | |
| PD1/GP71 | NB_LED2_C | |
| PD2/GP72/BUSS10 | NB_LED3_C | |
| GP22/SCK | LOW_PWR_1 | |
| VIDO5/GP27/SIN2 | LOW_PWR_2 | |
| PCIRST2#/GP11 | -PFMRST1 | |
| PCIRST1#/GP12 | -PFMRST2 | |
| 3VBSBW#/GP40 | CSI_F0 | BSEL166_1 |
| SUSC#/GP53 | CSI_F1 | BSEL166_2 |
| GP23/SI | BSEL166_3/CSISBSL | |
| VIDO0/GP20/CTS2# | CPUT_LED1_C | BSEL166_4 |
| GP65/VDDA_EN/GB_01 | MB_ID2 | |
| PD6/GP76/BUSS01 | MB_ID3 | |
| PD7/GP77/BUSS02 | MB_ID4 | |
| AFD#/GP86/SMB_C_R | ✗ PIN | FST_2X8 |
| INIT#/GP85/SMBD_M | SEC_2x8 | GT1REF_AD2 |
| ACK#/GP83 | DDR_LED1_C | |
| VIDO1/GP21/DCD2# | DDR_LED2_C | |
| STB#/GP87/SMB_C_M | DDR_LED3_C | |
| PWRON#GP44 | VCORE_OV1 | |
| PANSWH#/GP43 | PWRBTSW | |
| KDAT/GP61 | -PWRBTSW | |
| KCLK/GP60 | KDAT | |
| MDAT/GP57 | KCLK | |
| MACL/GP56 | MDAT | |
| GP66/VLDT_EN/GB_02 | NBT_LED1_C | MCLK |
| SVD/PCIRSTIN#/CIRTX/GP15 | PWM2_CR | |
| KDAT/GP61 | PWM2_CR | |
| GP67/CPU_PG/GB_03 | EN_LOADLINE | IT_GP67/-EN_PWM2 |
| SLIN#/GP84/SMBD_R | -EN_PWM2 | |
| PSI_L/FAN_CLT5/CIRRX2/GP16 | -THERM | |
| VIDO4/GP26/SOUT2 | DDR18V_PH2_EN | |
| VIDO2/FAN_TAC5/GP24/DSR2# | DDR18V_LED | |
| VIDO6/GP17/RI2# | 1_1V_PH_EN | |
| VIDO7/JP6/DTR2# | JP6 | |
| PD5/GP75/BUSS00 | SB_LED3_C | |



散熱模組料號:

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

| | 3 pin FAN control | 4 pin FAN control | FAN speed | Controller |
|---------|-------------------|-------------------|---------------|------------|
| CPU FAN | FANPWM1 | FANPWM3 | FANIO1 | IT8720 |
| | ICH_FAN_PWM2 | ICH_FAN_PWM0 | ICH_FAN_TACH0 | PCH |
| SYS FAN | FANPWM2 | N/A | FANIO2 | IT8720 |
| | ICH_FAN_PWM1 | N/A | ICH_FAN_TACH1 | PCH |
| PWR FAN | N/A | N/A | FANIO3 | IT8720 |
| | | | ICH_FAN_TACH2 | PCH |

| | | | |
|----------------------------|-------------------------|--|----------------|
| Gigabyte Technology | | | |
| Title | | | |
| TABLE LIST | | | |
| Size C | Document Number | | Rev |
| | GA-Z77X-UD3H | | 1.2 |
| Date: | Thursday, July 25, 2013 | | Sheet 41 of 41 |